AMC581

Xilinx Zynq® UltraScale+ FPGA, FMC Carrier, AMC

AMC581

Key Features

- Xilinx Zynq® UltraScale+ XCZU15EG FPGA
- 8 GB of 64-bit wide DDR4 Memory (single bank) with ECC
- MPSoC with block RAM and UltraRAM

Benefits

- FMC site on a single module AMC
- Zynq UltraScale+ MPSoC
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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AMC581

The AMC581 is an AMC FPGA Carrier with single FMC (VITA 57) interfaces. The AMC is compliant to AMC.1, AMC.2 and AMC.4 specifications. The unit has an onboard, re-configurable FPGA which interfaces directly to the AMC FCLKA, TCLKA-D, FMC DP0-9 and all FMC LA/HA/HB pairs.

The FPGA has interface to a single DDR4 memory channel (64-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The AMC is based on Xilinx UltraScale+ XCZU15EG MPSoC FPGA with single FMC site. The FPGA has 3528 DSP Slices and 746k logic cells. The XCZU15EG includes quad-core ARM application processor, dual-core ARM real-time processor and Mali™ graphics processing unit, as well as over 26 Mb of block RAM and 31 Mb of UltraRAM.

The module has onboard 64 GB of Flash, 128 MB of Boot Flash and an SD Card as an option.

Figure 1: AMC581

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Block Diagram

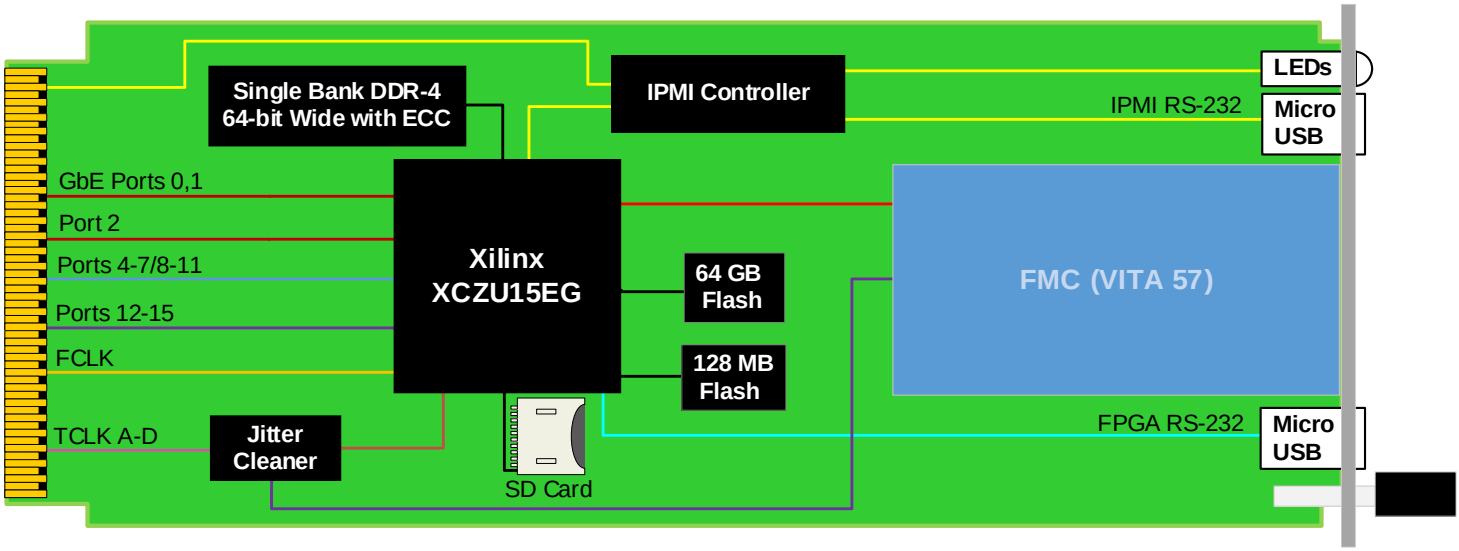


Figure 2: AMC581 Functional Block Diagram

Front Panel

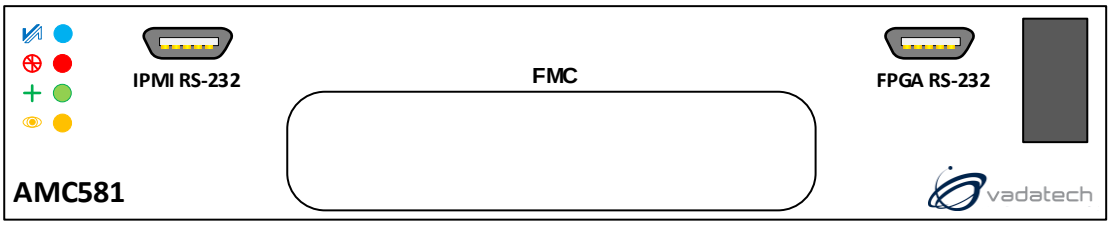


Figure 3: AMC581 Front Panel

Specifications

Architecture		
Physical	**Dimensions**	Single module, full-size
		Width: 2.89” (73.5 mm)
		Depth 7.11” (180.6 mm)
Type	**AMC FPGA Carrier**	Xilinx Zynq® UltraScale+ with FMC site
Standards		
AMC	**Type**	AMC.0, AMC.1, AMC.2 and AMC.4
Module Management	**IPMI**	IPMI v2.0
GbE	**Lanes**	Port 0 and 1
PCIe	**Lanes**	x4 (4-7/8-11) or x8 (4-11) and additional Ports on 12-15. (ZU15 - No hard-core PCIe)
10GbE/40GbE/SRIO		4-7, 8-11 and additional Ports on 12-15
Configuration		
Power	**AMC581**	~25W (FPGA load dependent and no FMC)
Environmental	**Temperature**	See Ordering Options and Environmental Spec Sheet
		Storage Temperature: –40° to +85°C
	Vibration	Operating 9.8 m/s^2 (1G), 5 to 500 Hz on each axis
	Shock	Operating 30G on each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	**Interface Connectors**	Single FMC Slot
		Dual micro USB for RS-232 (management and CPU)
	LEDs	IPMI management control
		Debug (user defined) LED
	Mechanical	Hot-swap ejector handle
Software Support	**Operating System**	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

AMC581 – A0C-DEF-G0J

A = Ports 12-15 to FPGA	D = SD Card	G = Clock Holdover Stability
0 = Not routed 1 = Routed as SERDES	0 = No SD Card 1 = 32 GB	0 = Standard (XO) 1 = Stratum-3 (TCXO)
	E = FPGA Speed	
	1 = Reserved 2 = High 3 = Highest	
C = Front Panel	**F = PCIe Fabric***	**J = Temperature Range and Coating**
1 = Reserved 2 = Mid-size 3 = Full-size 4 = Reserved 5 = Mid-size, MTCA.1 (captive screw) 6 = Full-size, MTCA.1 (captive screw) 7 = Mid-size, MTCA.1 (single captive)	0 = No PCIe 1 = PCIe on Ports 4-7 2 = PCIe on Ports 8-11 3 = PCIe on Ports 4-11	0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane** 7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic**

Notes: *ZU15EG does not have a hard-core PCIe IP block within reach of backplane PCIe. Customers must purchase a soft core PCIe IP block; please refer to Xilinx website.

.....**Conduction cooled, temperature is at edge of module. Consult factory for availability

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Related Products

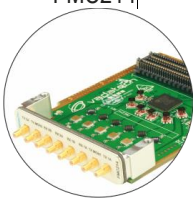
VT813

- MTCA.4 Chassis Platform with rear I/O
- 19” x 8U x 14.9” deep (with handles 16.23” deep)
- Full redundancy with dual MTCA Carrier Hubs

AMC592

- AMC FPGA carrier for FMC per VITA 57
- Xilinx UltraScale™ XCKU115 FPGA
- Supported by DAQ Series™ data acquisition software

FMC214



- Dual complete transceiver signal chain solution using Analog Devices AD9361 transceiver
- Frequency range 70 MHz to 6 GHz with instantaneous bandwidth from 200 kHz to 56 MHz
- MIMO transceiver is Time Domain Duplex (TDD)

Contact

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ALLIANCE PROGRAM CERTIFIED

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