VPX555

High-Speed ADC/DAC with Zynq+ and UltraScale+ FPGA with in 6U VPX

VPX555

Key Features

- Xilinx Virtex UltraScale+ XCVU13P FPGA
- Xilinx Zynq UltraScale+ XCZU4CG FPGA
- High speed ADC/DAC utilizing 3x Analog Device AD9081
- Synchronized 12 channel DAC/ADC
- RF DAC at 12 GSPS 16-bit
- RF ADC at 4 GSPS 12-bit
- All RF thru VITA 67.2 connectors
- Multi-board synchronization capable
- 8 GB of DDR-4 Memory to each FPGA
- 64GB of SSD
- Health Management through dedicated Processor with Tier-2 support

Benefits

- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™

vadatech
THE POWER OF VISION

VPX555

The VPX555 is a 6U VPX module with Virtex UltraScale+™ XCVU13P FPGA and a Zynq UltraScale+™ XCZU4CG FPGA in conjunction with three Analog Devices AD9081.

Each FPGA has 8 GB of DDR-4 memory. The Zynq+ PS side has a 64 GB of SSD for mass storage flash. The Zynq+ has a AXI-interface to the VU13P FPGA as well as high speed SERDES and a 1x PCIe.

Each AD9081 provides four DACs at 16-bit and four ADCs at 12-bit resolution. The 12 ADCs/DACs are fully synchronized to each other. The module receives a reference clock from the backplane as well as sync signals. This allows for the creation of a phase-coherent transceiver system spanning multiple VPX blades.

The health management is based on VITA 46.11 with Tier-2 support.

The unit is available in a range of temperature and shock/vibe specifications per ANSI/VITA 47, up to V3 and OS2.

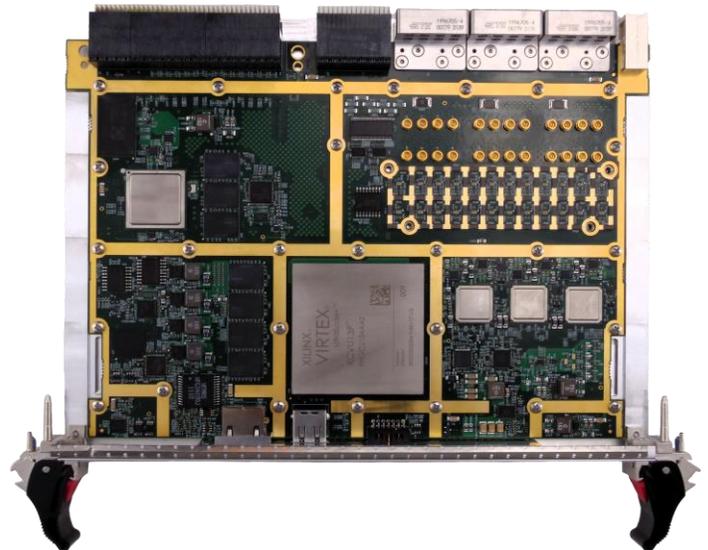Please contact VadaTech for details of Conduction Cooled versions.

Figure 1: VPX555

Figure 2: VPX555 Top View
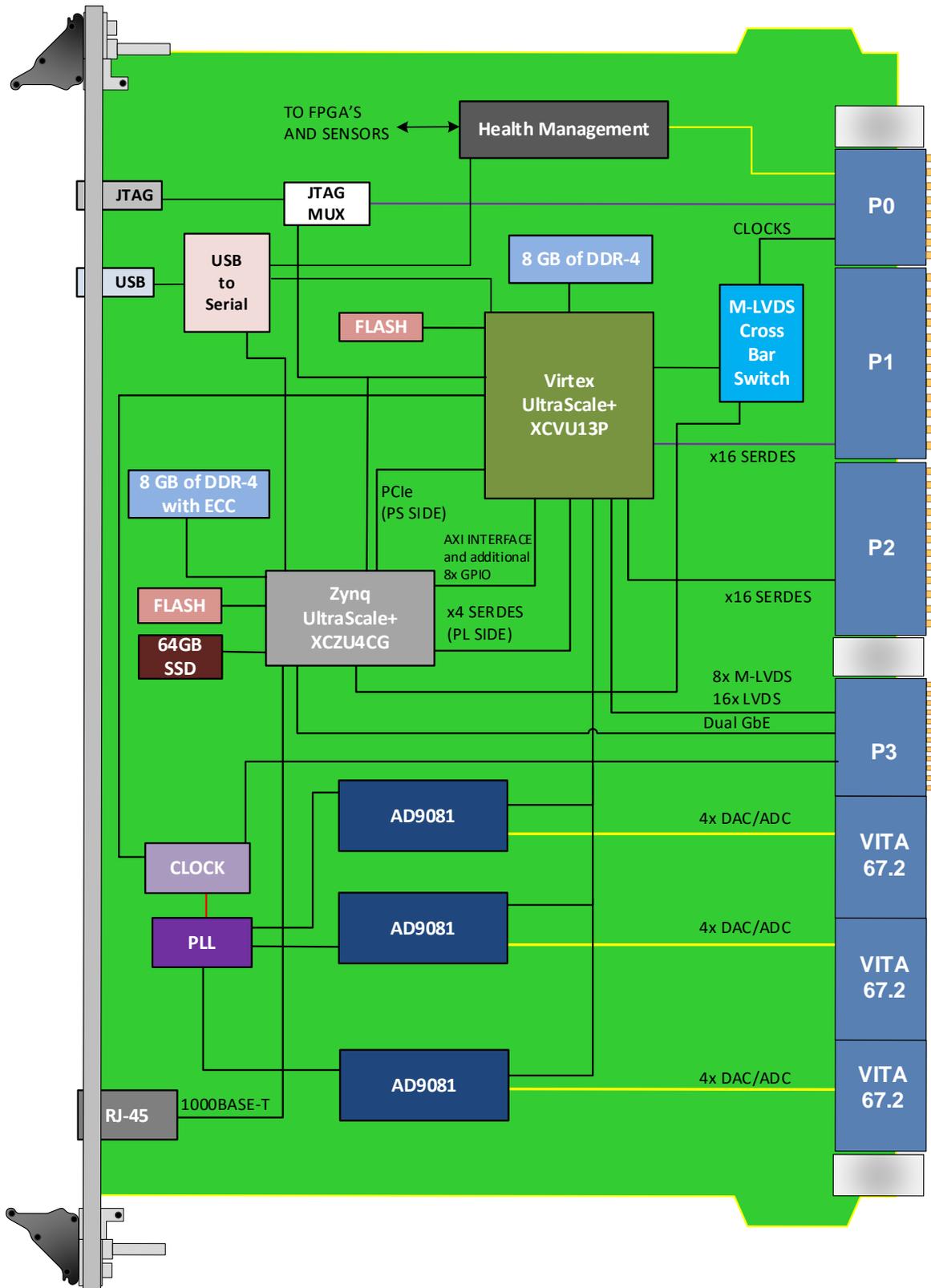

Figure 3: VPX555 Front Panel View

Block Diagram

Figure 4: VPX555 Functional Block Diagram

VPX555 – Virtex and Zynq UltraScale+™ FPGAs with High-speed ADC/DAC 6U VPX

Backplane Pinout

P3		
1	x8 M-LVDS to VU13P	
2		
3		
4		
5	x16 LVDS to VU13P	
6		
7		
8		
9		
10		
11		
12		
13	CLK / SYNC IN	
14		
15	Dual GbE	
16		
Row G	Management	

P2	
1	x16 SERDES to VU13P
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
Row G	Management

P1	
1	x16 SERDES to VU13P
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
Row G	Management

P6 — VITA67.2 x4 RX / x4 TX

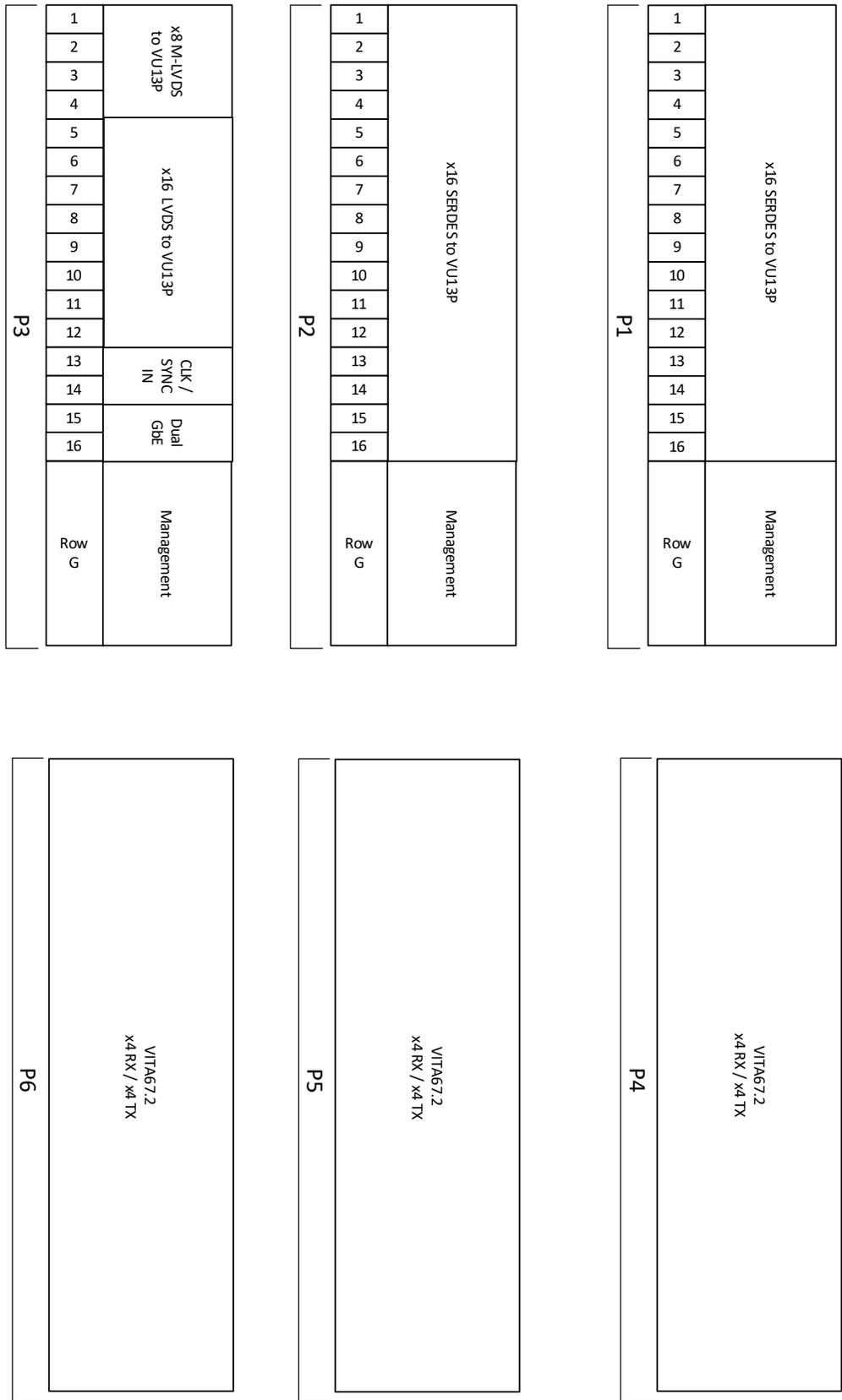**P5** — VITA67.2 x4 RX / x4 TX

P4 — VITA67.2 x4 RX / x4 TX

Figure 5: VPX555 Backplane Pinout

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high-speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

[Xilinx Vivado Design Suite](), [Xilinx System Generator for DSP]().

Specifications

Architecture			
Physical	**Dimensions**		6U, VPX
FPGA			Xilinx Virtex UltraScale™ VU13P and Zynq UltraScale™ ZU4CG
Configuration			
Power	**VPX555**		~100W (FPGA load dependent)
Front Panel	**JTAG**		JTAG header via front or P0
	USB		USB-to-Serial
	LEDs		User defined by the FPGA and Health Management
VPX Interfaces	**Slot Profiles**		See Ordering Options
	Rear IO		P1: x16 SERDES
			P2: x16 SERDES
			P3: M-LVDS, LVDS, Clocks, Dual GbE
			P4: VITA 67.2
			P5: VITA 67.2
			P6: VITA 67.2
Software Support	**Operating System**		Linux
Other			
MTBF		MIL Hand book 217-F@ TBD hrs	
Certifications		Designed to meet FCC, CE and UL certifications, where applicable	
Standards		VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty		Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX555 – ABC-D00-GHJ

A = RF Clock	D = FPGA Speed	G = Applicable Slot Profiles
0 = Rear P3 connector 1 = Reserved 2 = Reserved	1 = Reserved 2 = High 3 = Highest	0 = 5 HP, VITA 48.1
B = Front End Balun		**H = Environmental**
0 = Anaren 400MHz to 3GHz 1 = Reserved 2 = Reserved		See Environmental Specification
C = VPX Connector Type		**J = Conformal Coating**
0 = Standard 50u Gold Rugged 1 = KVPX Connectors		0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Notes:

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes:

*Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4)

VPX555 – Virtex and Zynq UltraScale+™ FPGAs with High-speed ADC/DAC 6U VPX

Related Products

VPX516

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX592

- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014

Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan

Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR

Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

Choose VadaTech

We are technology leaders

- First-to-market silicon
- Constant innovation
- Open systems expertise

We commit to our customers

- Partnerships power innovation
- Collaborative approach
- Mutual success

We deliver complexity

- Complete signal chain
- System management
- Configurable solutions

We manufacture in-house

- Agile production
- Accelerated deployment
- AS9100 accredited

vadatech
THE POWER OF VISION