VPX582

Integrated Octal RF Transceiver in for L1/L5 Band or Wider Freq 800MHz to 2.8GHz in 3U VPX

VPX582

Key Features

- Octal RF transceiver utilizing AD9371 and/or AD9375
- Xilinx UltraScale+ XCZU15EG FPGA
- 8 GB of 64-bit wide DDR-4 Memory with ECC to ARM
- 8 GB of 64-bit wide DDR-4 Memory to FPGA
- MPSoC with block RAM and UltraRAM
- L1/L5 Band Filter and Amplifier with option for 800MHz to 2.8GHz input without Filters
- Health Management through dedicated Processor

Benefits

- Integrated transceiver covering 300 MHz to 6 GHz
- Rx BW: 8 MHz to 100MHz
- Tx synthesis bandwidth (BW) to 250 MHz
- Reference design with VHDL source code speeds application development
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™

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VPX582

The VPX582 provides octal integrated RF transceivers based on Analog Device AD9371 or AD9375. The module is compatible with Analog Devices design tools. The RX RF front end is designed for the L1/L5 Band and it has a filter and amplifier per each RX input. The VPX582 comes with option for input RF of 800Mhz to 2.8GHz without the filters.

VPX582 is based on Xilinx UltraScale+ XCZU15EG MPSoC FPGA, which has 3528 DSP Slices and 746k logic cells. The XCZU15EG includes quad-core ARM application processor, dual-core ARM real-time processor and Mali™ graphics processing unit, as well as over 26 Mb of block RAM and 31 Mb of UltraRAM.

The Module routes its RF TX/RX to the front panel. The VPX582 has 8 TX/RX SERDES, Dual GbE as 1000Base-BX, Dual GbE as 10/100/1000Base-TX, x2 PCIe from PS, 8 LVDS (could be configured as singled ended), 16 +3.3V GPIO, CPU RS-232 and management RS-232 to the P1/P2 connector.

Each of the receiver side (RX) have an L1/L5 band filter followed by with an LNA (Low Noise Amplifier). Each of the transmitter side (TX) have the output go thru the L1/L5 band filter.

The ARM processor interface to the 8GB of DDR-4 memory with ECC and the FPGA interfaces to a single DDR4 memory channel (64-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The module has on board 64 GB of Flash and 128 MB of Boot Flash.

Figure 1: VPX582

Figure 2: VPX582 without front panel

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Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Block Diagram

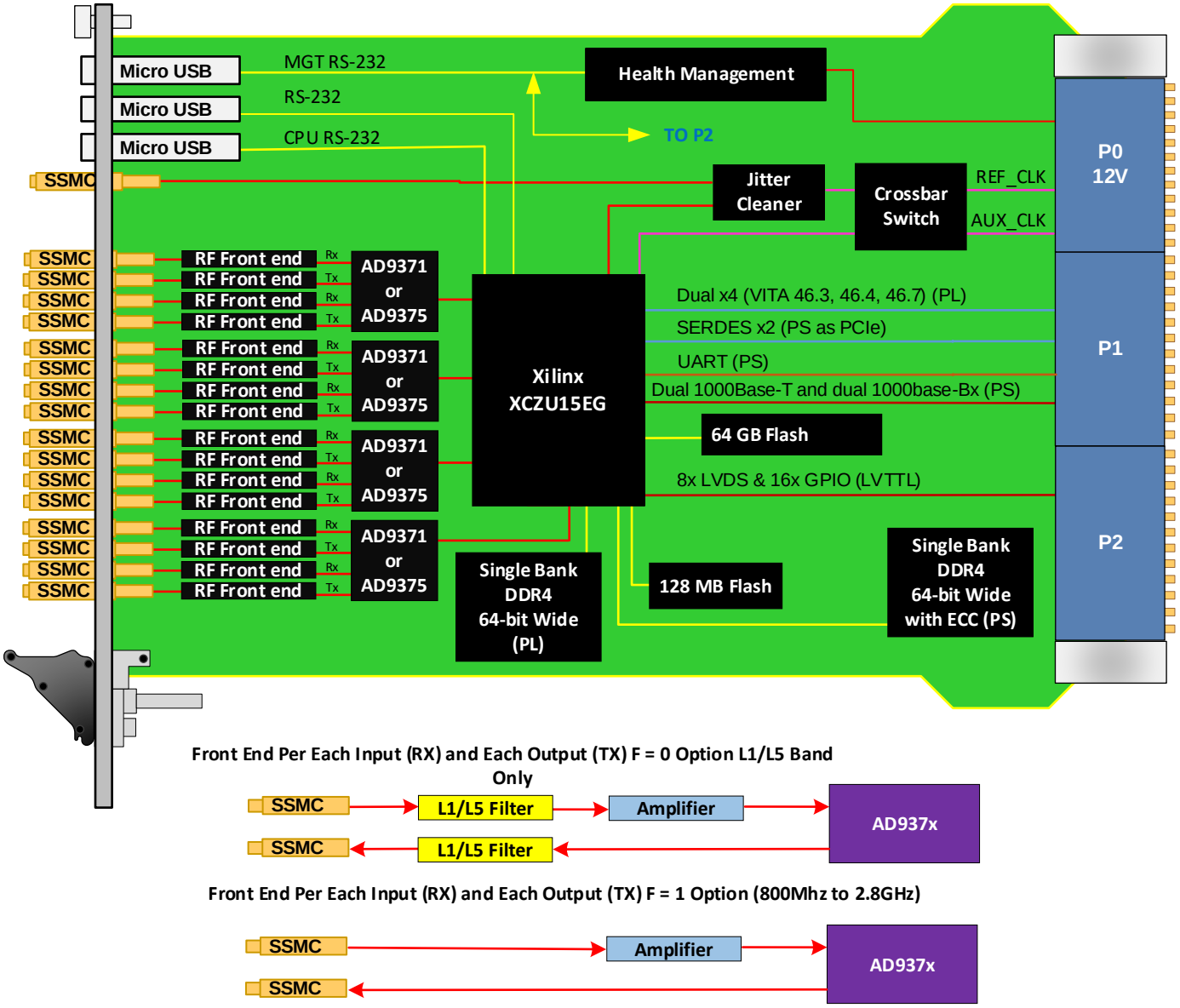

Figure 3: VPX582 Functional Block Diagram

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
Type	**Controller**	OpenVPX payload module with Health Management
Standards		
VPX	**Type**	VITA 46.x
VPX	**Type**	VITA 65 OpenVPX
Module Management	**IPMI**	IPMI v2.0
Configuration		
Power	**VPX582**	~50W (FPGA load dependent)
Front Panel	**Interface Connectors**	16 SSMC RF RX/TX and one SSMC for the front clock input
		Triple Micro USB as RS-232
	LEDs	User defined by the FPGA and Health Management
VPX Interfaces	**Slot Profiles**	See ordering options
	Rear IO	Health Management, Clock and JTAG on P0
		x8 SERDES on P1
		x2 PCIe and quad GbE from PS to P1
		8 LVDS or 16 singled ended with additional 16 +3.3V I/O to P2
		RTM management on P1/P2
Software Support	**Operating System**	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX582 – ABC-DEF-GHJ

A = RS-232 Level Shifter for P1 G9/G11	D = FPGA Speed	G = Slot Profile
0 = Installed (TX/RX are level shifted per RS-232 specification) 1 = Not Installed	0 = Reserved 1 = High 2 = Highest	0 = 5 HP, VITA 48.1
B = RF Transceiver	**E = Dual 1000BASE-T to P1**	**H = Environmental**
0 = AD9371 1 = AD9375	0 = Isolated Magnetic (standard option) 1 = Without Magnetic utilizing Capacitor Isolation	See Environmental Specification Table below
C = VCXO	**F = Front End RF**	**J = Conformal Coating**
0 = 122.88 MHz 1 = 100 MHz	0 = L1/L5 Band 1 = 800Mhz to 2.8GHz (no filter)	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Notes:
For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX004

- Unified 1 GHz quad-core CPU for, Shelf Manager, and Fabric management
- Automatic fail-over with redundant VPX004
- 1GbE base switch with dual 100/1000/10G uplink

VPX752

- 6U VPX module Intel 5th Generation Xeon-D SoC
- PCIe Gen3 x 16 (dual x8 or Quad x4)
- Quad 10GbE XAUI

VTX870

- Open VPX benchtop development platform
- Dedicated Switch/management slot
- Up to five 3U VPX payload slots

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