VT981

3rd Generation RFSoC w/ XCVU13P FPGA and RF/IF carrier

VT981

Key Features

- 8 ADC / 8 DAC simultaneous processing
- 3rd Generation Xilinx RFSoC XCZU47DR
  - 16GB of DDR4
- Suitable for 5G, 4G, LET and SDR deployment
- FPGA data processing w/ Xilinx Virtex UltraScale+ XCVU13P
  - 16GB of DDR4
- FMC+ socket for addition RF and I/O
  - The FMC+ could extend beyond the FMC+ in length for added real estate (up to XMC size is supported)
- Accommodate 3rd party RF/IF daughter card
  - Accomplished thru an FMC connector to the RF Module
- Clock and Timing Synchronization to the RF/IF

Benefits

- Design utilizes proven VadaTech subcomponents and engineering techniques
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply by industry leader
- AS9100 and ISO9001 certified company

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The VT981 is a complete data acquisition and processing platform capable of synchronous sampling, suitable for customer development of custom RF front end. It has 8 channels ADC and 8 channels DAC embedded in the 3rd generation RFSoC XCZU47DR with bandwidth up to 800MHz from DC to 6GHz. The RFSoC provides clock and frame synchronization signals to the RF/IF Daughter Card, the DSP FPGA, and external Control Module.

The RFSoC has 8GB 64-bit DDR4 with ECC to the CPU and 8GB 64-bit DDR4 to the Fabric side. The Xilinx ZCVU13P has 16GB 64-bit DDR4 (two banks of 8GB) on-board memory. Both XCZU47DR and the XCVU13P have JTAG and serial via the front dual USB connectors.

The RFSoC interface includes CPRI over SFP+ on the front panel and the FPGA XCVU13P supports six 100GbE interfaces via QSFP28 on the front panel.

The VT981 has a Layer 2 Managed Gigabit Ethernet Switch with dual GbE (RJ-45) and single 10GbE (SFP+) interfaces to the front panel, providing interconnection among the subsystems.

VT981 has an option for an FMC+ module which interfaces to the VU13P FPGA. The module mounted here can be larger than the FMC+ specification to extend the area available for components, allowing up to an XMC module size. The XCZU47DR RF is routed to an interface connector with an additional FMC style connector for control to a customer RF front-end module.

The VT981 has a dedicated CPU for health management. The health management CPU monitors the sensors in the chassis and controls the cooling dynamically. The cooling is from right to left.

VadaTech could work with customer to develop the front RF module or customer could make their own front RF module which mates to the VT981 motherboard. Currently VadaTech has developed the DA358 which has the MARKI balun with digital I/O (i.e. RS-422, +3.3V and +5v) for control of external devices.

The chassis mounting provision allows the unit to be in a 19” rack or ceiling mounted.

Figure 1: VT981

Block Diagram

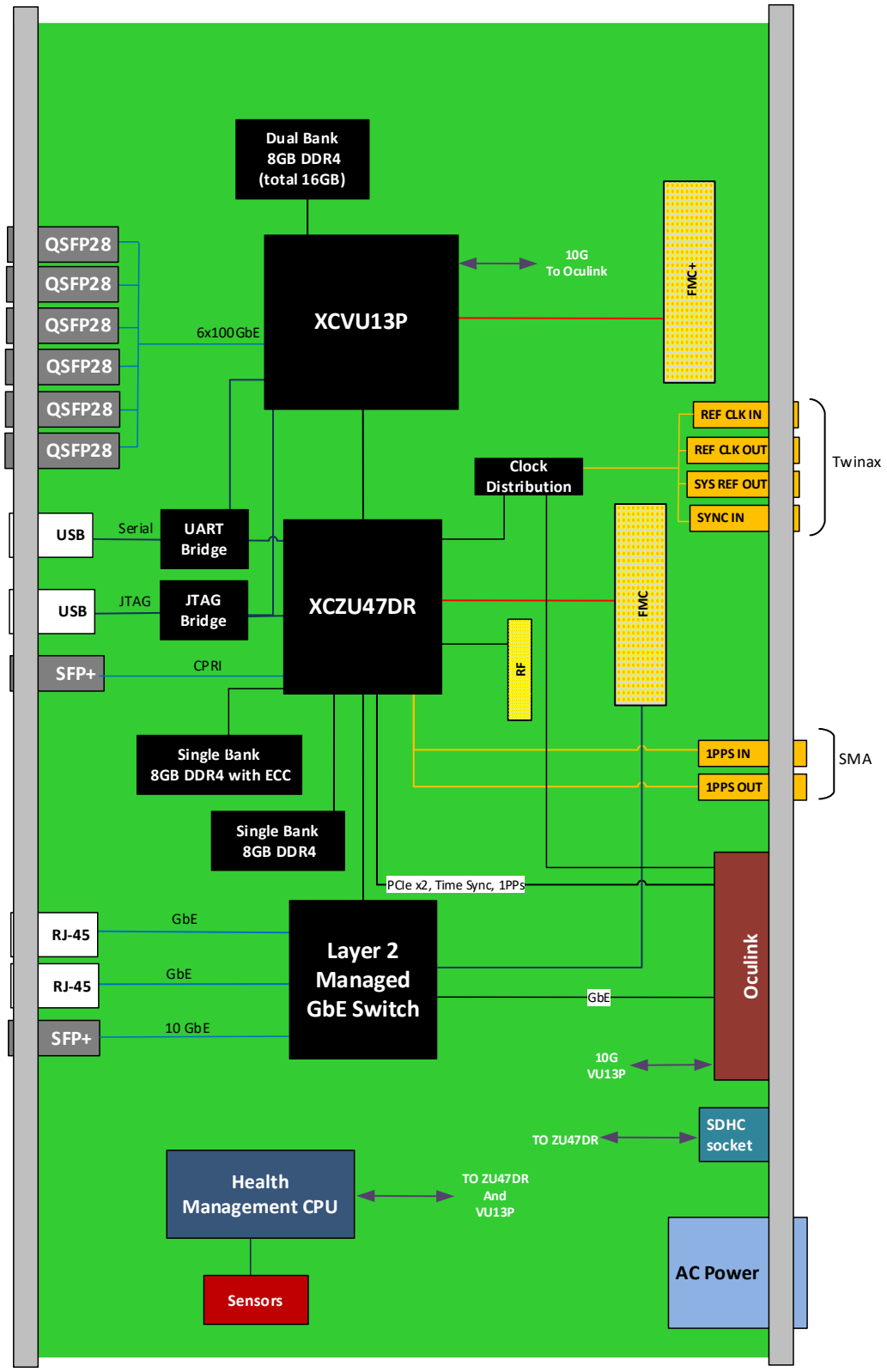

Figure 2: VT981 Functional Block Diagram

Chassis

Figure 3: VT981 Top View

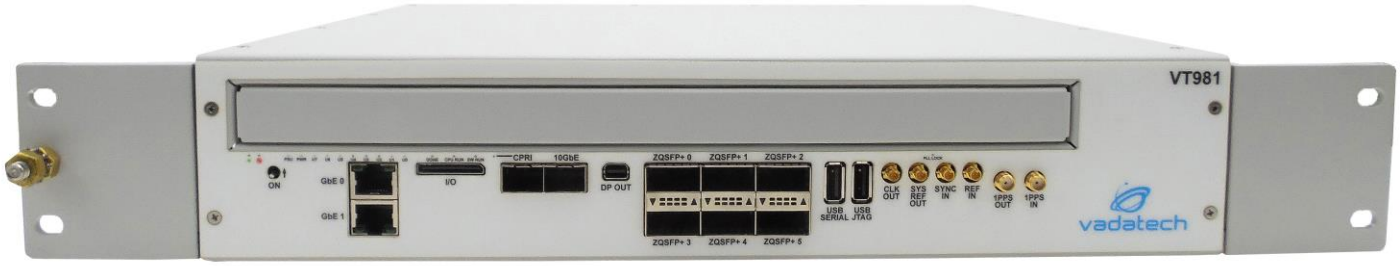

Figure 4: VT981 Front View

Figure 5: VT981 Rear View

Chassis (cont.)

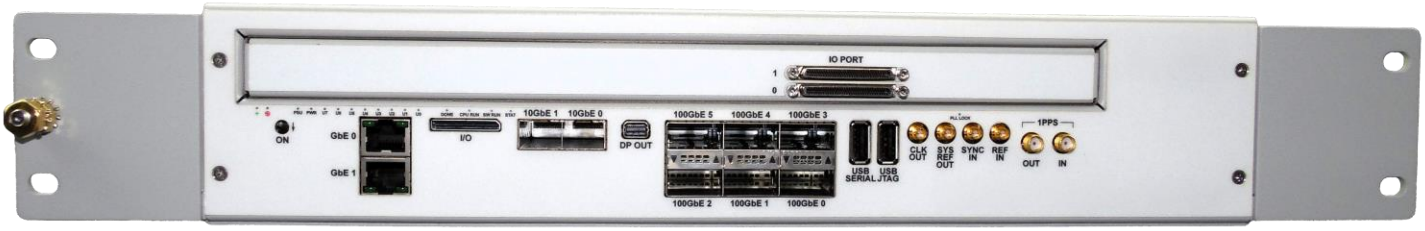

Figure 6: VT981 G = 1 Front View

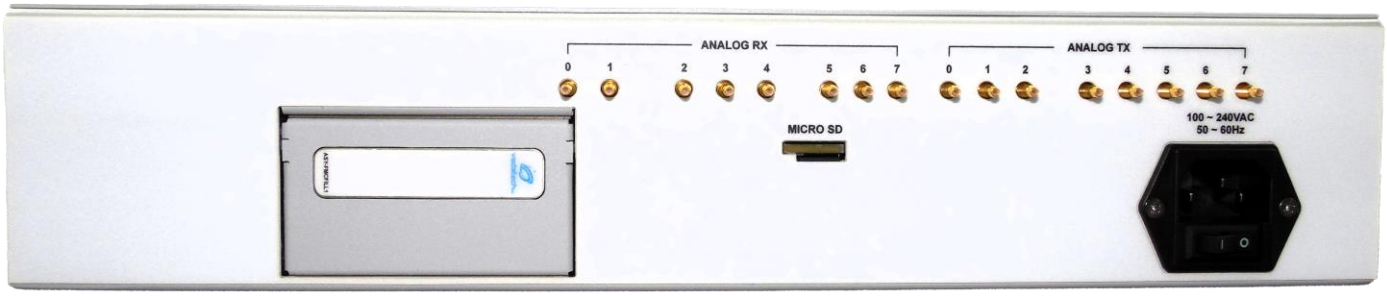

Figure 7: VT981 G = 1 Rear View

Specifications

Architecture		
Physical	**Dimensions**	Width: 14.4”
		Depth: 10.9”
		Height: 2.65”
Type	**Chassis**	ADC/DAC Data Acquisition and signal processing
Configuration		
Power	**VT981**	~130W FPGA dependent load and without the RF module
Environmental	**Temperature**	Operating Temperature: -5° to +55°C
		Storage Temperature: –40° to +85°C
	Vibration	Operating 9.8 m/s^2 (1G), 5 to 500Hz on each axis
	Shock	Operating 325G/2 ms, 160G/1 ms
	Relative Humidity	5 to 90% non-condensing
Rear Panel	**Interface Connectors**	110-240VAC 50-60Hz Mains inlet (400W)
		2x SMA and 6x TWINAX
Front Panel		2x SFP+
		2x RJ-45 for GbE
		2x USB for Serial and JTAG
		6x QSFP28 for 100GbE
		Single x8 OcuLink
Software Support	**Operating System**	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	One (1) year, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VT981 – AB0-DE0-G0J

A = QSFP28 Transceiver*	D = RF FPGA speed	G = Front RF Module
0 = No TXCVR 1 = 100GbE 100m SWDM4 2 = 100GbE 100m SR 3 = 100GbE 2km CWDM4 4 = 100GbE 10km eCWDM4 5 = 100GbE 10km LR 6 = Reserved	0 = Low 1 = High 2 = Reserved	0 = None 1 = Balun (Marki BAL-006SMG) with Digital I/O (RS422, +3.3V and +5V) via VHDCI style connectors (VadaTech DA358 module) 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved
B = Clock Connection	**E = VU13P speed grade**	
0 = EXT_SYSREF output 1 = eCPRI Clock input	1 = High (-2) 2 = High (-2LE) 3 = Highest (-3)	
		J = Temperature Range and Coating
		0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic

*Quantity six will be delivered with module

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Related Products

AMC521

- Sixteen channel ADC 16-bit @ 250 MSPS (TI ADS42JB69)
- Eight channel SAR, ADC 16-bit @ 650 KSPS simultaneous (TI ADS8568)
- Interface to the FPGA is via JESD204B

AMC524

- Quad ADC 16-bit @ 125 MSPS (AD9653)
- Dual DAC 12-bit @ 2.5 GSPS (DDS AD9915)
- Artix-7 FPGA with dual banks of DDR3, 2 GB total

AMC526

- Dual ADC 12-Bit @ 2.6 GSPS (AD9625) in single module, mid-size
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- Quad bank QDR-II+ memory (576 Mb total) and 1 Gb DDR3

Contact

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