XMC500

XMC Xilinx Kintex Ultrascale+ FPGA with onboard PLL and front optical option

XMC500

Key Features

- Single width XMC per VITA 42
- Xilinx Kintex Ultrascale+ (XCKU11P)
- On board PLL to sync to 1PPS and/or any input frequency (1MHz to 100MHz) for MGT bank synchronization
- Front I/O with 12 TX/RX optics via MTP/MPO
- Optical up to 25G per lane to the front (option to run as 100G ethernet or any other protocol)
- Dual bank of DDR-4 with total of 8GB of memory
- I/O to the XMC P16 per VITA46.9 as X24s+X8d+X12d

Benefits

- Design utilizes proven VadaTech subcomponents and engineering techniques
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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XMC500

The XMC500 is an XMC module per VITA 42 specification and based on the Xilinx Kintex Ultrascale+ FPGA XCKU11P. The XMC500 interfaces to the host via x8 PCIe Gen3 (other protocols such as 1G/10G/40G, Aurora, SRIO, etc. are possible by programming the FPGA).

The XMC500 has dual bank of DDR-4 memory (32-bit wide) for a total of 8GB of memory.

The module follows the VITA 46.9 and routes I/O to XMC P16 as X24s+X8d+X12d. Two of the X24s are used for the 1PPS and sine wave input as sync clock to the on board PLL. There are six LVDS input/output (could be configured in any combination as single ended +1.8V) and ten GPIO +3.3V. Ten of the X12d are high speed SERDES that connect directly to the MGT Bank of the FPGA.

The 10 high speed SERDES going to the P16 could be configured for PCIe or non-PCIe protocols. There are two hard core PCIe and some of the valid PCIe configuration are show below:

- No PCIe
- x8 PCIe and x2 PCIe
- x4 PCIe, x4 not PCIe and x2 PCIe
- x8 not PCIe and x2 PCIe

There are many other combinatorial to take advance of smaller PCIe lanes to add more lanes to the non-PCIe protocols such as:

- x1 PCIe, x7 not PCIe, x1 PCIe and x1 not PCIe

Please contact VadaTech for other configurations.

The module has an option for the front panel Optical via MTP/MPO optics which can operate up to 25G per lane. This allows operations such as 100Gb ethernet. Since the FPGA is programable any protocol could be run on these lanes with mix and match including PCIe, Aurora, etc.

The XMC500 has an on board PLL which can generate any frequency to the MGT banks. The PLL can lock into a 1PPS or 10Mhz (or any sine wave input up to 300MHz) clock. The sync clocks have their input thru the front panel or thru the P16 connectors. User can select the sync input and the priority. The XMC500 could still operate and generate any clock to the MGT without any sync reference clock.

The PLL has hitless fail over its input sync clocks. The PLL has an OCXO for stability reference and XO as the jitter reference.

The module is available in both air cooled and conduction cooled versions.

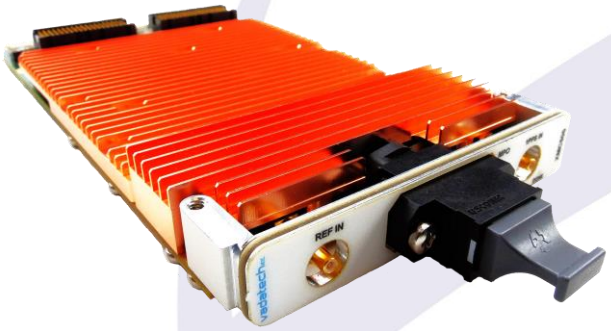

Figure 1: XMC247

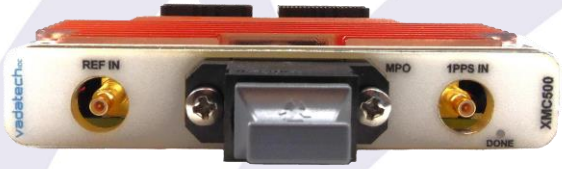

Figure 2: XMC247 Front View

Figure 3: XMC247 Top View

Block Diagram

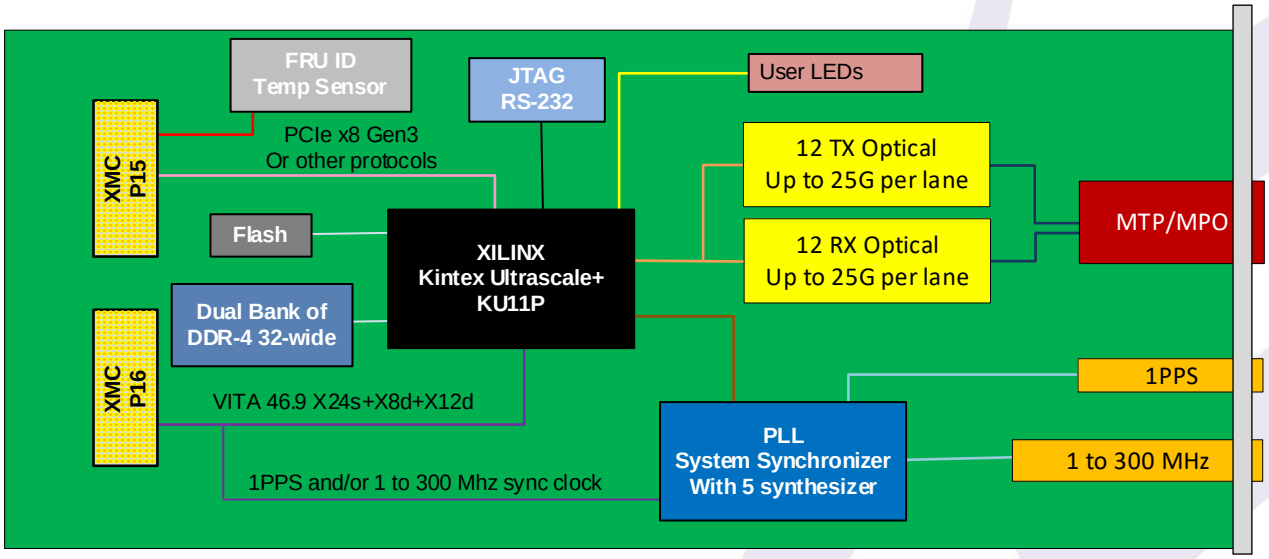

Figure 4: Functional block diagram

Specifications

Architecture		
Physical	**Dimensions**	Single-Width, per VITA 42.0 specification
Type	**XMC FPGA**	Kintex Ultrascale+
Standards		
XMC	**Type**	PCIe/1G/10G/40G/100G, Aurora, SRIO , etc.
Module Management	**Sensors**	FRU info and Temp sensor
Configuration		
Power	**XMC500**	25W FPGA load dependent
Environmental	**Temperature**	See Ordering Options and Environmental Spec Sheet
Front Panel	**Interface Connectors**	To P16 of XMC as well as front I/O
	LEDs	Total of 8 user defined
Software Support	**Operating System**	Agnostic
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

XMC500 – ABC-0EF-0HJ

A = FRONT I/O		
0 = Not installed 1 = 25G per lane optical MTP/MPO 2 = 10G per lane optical MTP/MPO		
B = XMC interface to host	**E = FPGA Speed**	**H = Environmental**
0 = Other protocols 1 = PCIe	1 = Reserved 2 = High 3 = Highest	See Environmental Specification
C = XMC Connectors	**F = XMC P16 PCIe Config (10 SERDES)**	**J = Conformal Coating**
0 = VITA 42 1 = VITA 61	0 = No PCIe 1 = x8 PCIe and x2 PCIe 2 = x4 PCIe, x4 not PCIe and x2 PCIe 3 = x8 not PCIe and x2 PCIe 4 = Reserved 5 = Reserved	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes:

*Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX762

- 6U VPX module Xeon-D SoC (Skylake-D) 6th-Generation
- Single XMC site with I/O expansion going to P5/P6 per VITA46.9 Pin Field P5W1-P64s+X12d+X8d
- PCIe Gen3 x16 (bifurcation to dual x8 or quad x4)

VPX752

- 6U VPX module Intel 5th Generation Xeon-D SoC
- Single XMC site with I/O expansion going to P5/P6
- PCIe Gen3 x16 (dual x8 or quad x4)

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014
Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan
Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR
Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

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