Solution Brief

IRIG-B/GPS timestamped 56Gsps digitizer with dual 40G extension

VadaTech customers target the next generation of data processing embedded systems. They require our support for them to develop algorithms using the most advanced technology embedded in a form factor (format) that they can deploy outside a laboratory environment.

This Solution Brief introduces how VadaTech application team has helped different customers reach an unprecedent level of development capability. The integration of building blocks includes a 56Gsps high-speed digitizer, PCIe Gen3/40G backplane, network interfaces and modulated timing solutions. The first solution is integrated in a 5U high (8.75″) chassis and the second 1U high (1.75″) chassis, both for standard 19″ racks.

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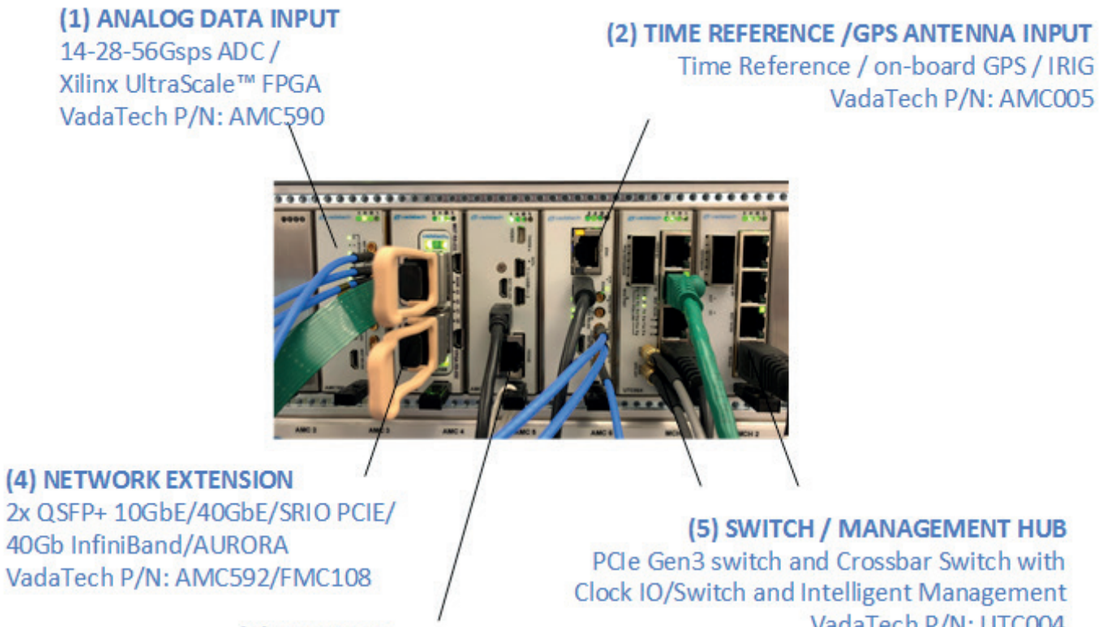
MAIN FUNCTIONS OF THE 5U SYSTEM



VadaTech provides support for the assembly of the module into a CuSTom (CST) integrated system with advanced functions. This system includes:

1/ On-board DDR4 FIFO with 24G-samples snapshot storage

2/ Time synchronization, Time Trigger and Timestamp based on GPS

3/ Clock/Acquisition control and configuration via Intel host CPU

4/ Transfer of snapshot to the Host via PCIe Gen3 over the backplane

5/ Provide capability for future network extension via the dual QSFP+ interface

(1) 14 or 28GSPS DIGITIZER to FPGA and DDR4

The analog signal generated by the customer's application (sensor) is digitized at 14 or 28 Gsps (Giga-samples per seconds) and transferred over High-Speed Serial Interface protocol (HSSI) to the FPGA FIFO memory and DDR4 FIFO embedded in a unique module (AMC590). Due to DDR4 inherent write speed it's not possible to use the ADC in 56Gsps mode with the DDR4 FIFO.

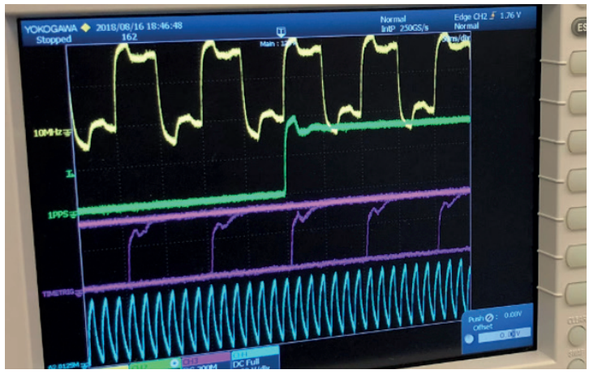
The DDR4 FIFO is implemented in the FPGA with priority to write over read since the writes are real-time and the reads are deferred-time in the FPGA reference design. This provides at least 24G-samples snapshot storage capability.

FPGA must be speed grade -3 for this application (standard would be -2).

For the purpose of testing the module with a signal generator it is possible to connect the single-ended output from the signal generator to the differential inputs of the AMC590 using an external high frequency balun.

(2) GPS 1PPS, 10MHz and TIMESTAMP

The GPS antenna is connected to the AMC005 front panel. The embedded GPS provides the1PPS reference and time which is then IRIG-modulated in the AMC005. The 1PPS is regenerated together with a disciplined 10MHz. The two clocks and time-trigger are routed from the AMC005 to the AMC590 via the backplane and the configurable clock crossbar switch (embedded in the UTC004 MCH). The AMC590 is configured to use the reference clocks to generate its ADC sampling clock locally, to start on time-trigger event and to use the timestamp in the FPGA to add time information to the ADC samples.



(3) HOST CPU

The CPU includes the host software tools for the clock module (AMC005) and the data acquisition module (AMC590) over PCIe Gen3x4. The host is able to read the 24G-samples snapshot from the DDR4 FIFO located on the AMC590 via the same protocol.

(4) FPGA with QSFP+ extension

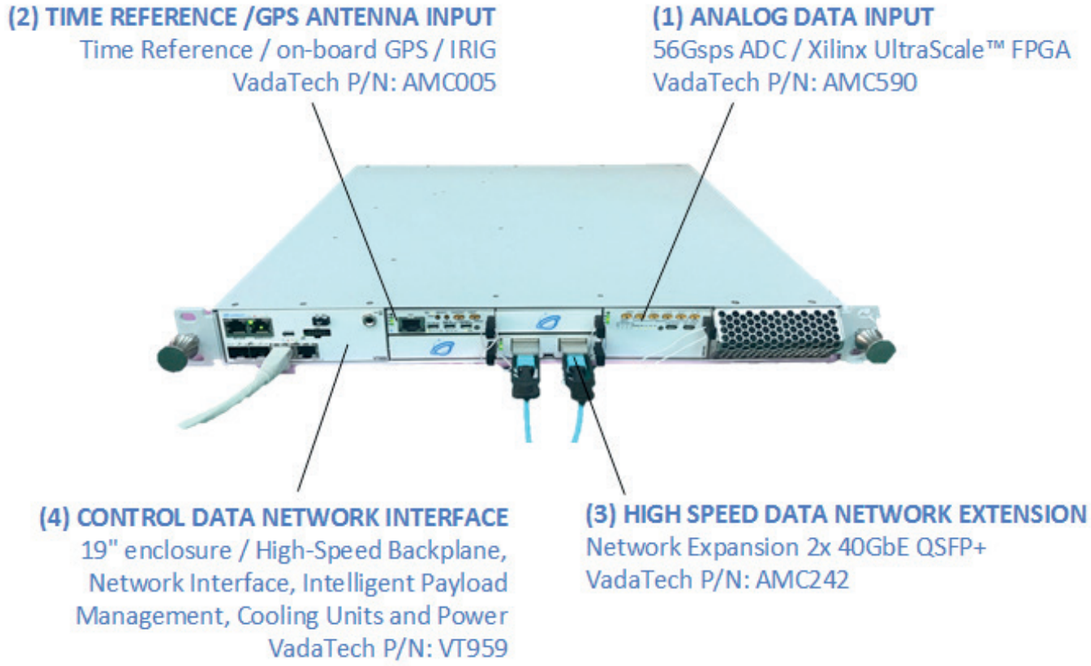
The dual QSFP+ network extension (FMC108) is installed on the AMC592 with Kintex Ultrascale FPGA. The crossbar switch and the backplane topology provide a total of 8x high-speed SERDES lanes connected between the AMC592 FPGA and the AMC590 FPGA. Customer has the choice of protocol implementation between 10GbE/40GbE/SRIO PCIE/40Gb InfiniBand or AURORA.

(5) Switch and Management HUB

The modules are linked to the switches via the backplane in a dual-star topology. The switches are located in the MCH (UTC004). The switch is selected based on the high-speed communication protocol preferred. In this case the first switch is a PCIe Gen3 (for the connection to the Intel Host) and the second is a Crossbar switch (for the network extension to the dual QSFP+).

Additional management functions such as power allocation, cooling unit control and sensors reading are provided by the MCH.

MAIN FUNCTIONS OF THE 1U SYSTEM



VadaTech solutions are based on a standard and modular architecture which allows to scale the solution and comply with the performances, size and budget available. Our customer needed a smaller footprint and tighter budget but required a higher network extension bandwidth for data processing in an external server. This deliverable allowed the customer to:

1. Connect the sensor analog signal to capture a snapshot of that data in the ADC and transfer it into an internal FPGA FIFO memory. After the snapshot is captured, the data can be transferred from the FIFO to an external PC for subsequent analysis with Matlab or some other third-party ADC analysis software

2. Connect a timing reference or GPS antenna, and use the 1PPS, IRIG-B and Timestamp signals regenerated and routed to the FPGA for data timestamping and disciplined data acquisition

3. Connect a loop-back test or an external server to the FPGA via the high-speed interface (40G Base-R IP, backplane, transceivers and fibre cables)

4. Receive alarms and status from the intelligent system manager (power, cooling, alarms, sensors reading)

(1) 56GSPS DIGITIZER to FPGA

The analog signal generated by the customer's application (sensor) is digitized at 56Gsps (Giga-samples per seconds) and transferred over High-Speed Serial Interface protocol (HSSI) to the FPGA FIFO memory embedded in a unique module (AMC590).

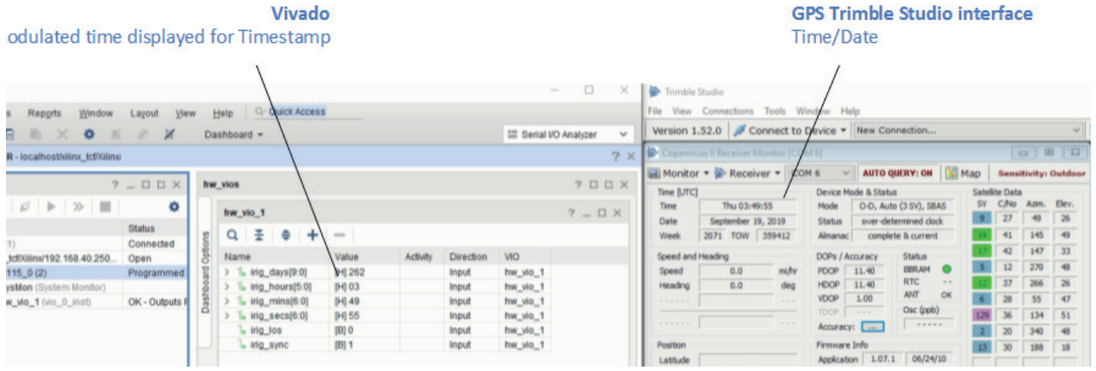
Key Features:

- Capability to setup the data acquisition mode in single-channel @56Gsps or dual-channels @28Gsps
- ADC initialization, internal calibration and transfer to the FPGA are fully included in the Board Support Package (code) supplied by VadaTech.

The modules integrated in the 5U chassis have dedicated separate airflow channels. In a 1U chassis the airflow passes through the modules in series so it's important to use the space available and maximize the cooling of the hottest components. For this purpose we use the 8HP for the AMC590 with larger heatsink compared to the solution developed in the 5U chassis.

(2) GPS 1PPS, IRIG-B and TIMESTAMP

The functions are generally the same as for the 5U system with the difference that the customer used IRIG modulation/demodulation for the timestamp. Another difference is the clock crossbar switch is embedded in the chassis (not within the removable UTC004). The AMC590 is also configured to use the reference clocks to generate its ADC sampling clock locally, and to IRIG-decode the GPS timestamp in the FPGA to add time information to the ADC samples.



(3) FPGA with 40GbE Base-R, Transceivers and Fibre

The backplane provides 2x 40GbE between the AMC590 FPGA and the AMC242 dual QSFP+ extension.

VadaTech's application team has installed the Xilinx® LogiCORE™ IP 40G Ethernet solution which provides the AMC590 FPGA with a 40 Gbps Ethernet Media Access Controller BASE-R mode (license purchased by the customer separately - contact Sales for details).

High-end QSFP+ transceivers are setup with appropriate tuning to provide the best bandwidth. The fibre cable can be used as a loop back to demonstrate the performances of the system. This allows easier integration with a 3rd party server onsite in a second phase.

VadaTech has the building blocks to support 5x100GbE (contact VadaTech Sales for details).

(4) Management, Power, Cooling

VadaTech products are compliant with the industry open standards of choice and quality requirements in order to provide the end-user with Scalability, Interoperability and Affordability.

The power-module and cooling-units with air-filter are removable and replaceable on the field.

The intelligent management processor provides access to sensor readings, automatic air-flow adjustment and alarm reports.

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Best Industry Standards

Designed and manufactured in the USA, we utilize open-standard platforms from VITA and PICMG for modularity and scalability, lowering your CAPEX and risk.

AS9100 is the international Quality Management System standard for the Aviation, Space and Defense (AS&D) industry.

VadaTech has in-house certification for IPC610 acceptability of electronic assembly, IPC620 acceptability of cable harness and wire assembly and IPC J-STD-001F manufacturing and soldering process for electronics. VadaTech is an IPC Member. www.ipc.org

PICMG is the leading standards development organization in the embedded computer market. PICMG has developed standards such as AdvancedTCA®, MicroTCA® CompactPCI® or COM Express®.

FPGA Mezzanine Card, or FMC, as defined in VITA 57, provides a specification describing an I/O mezzanine module with connection to an FPGA. VadaTech is a Member of the FMC Marketing Alliance. VITA VPX is a broadly defined technology utilizing the latest in a variety of switch fabric technologies in 3U and 6U format blades.

Certified Alliance Partners have met vigorous training requirements, maintain a deep understanding of Xilinx technology, and offer a high level of technical expertise to global customers.

The Intel FPGA Design Solutions Network (DSN) is an ecosystem of experienced, independent worldwide companies that provide customers with valuable products and services that complement Intel FPGAs, SoCs, Structured ASICs, and Intel Enpirion® Power Solutions. VadaTech is Gold member of the Intel DSN.

Analog Devices PartnerZone is where you can go to easily connect with electronic design service companies who are members of Analog Devices Design Partner Network. VadaTech is listed in Analog Devices Engineering PartnerZone. https://ez.analog.com/

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