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White Paper

A Scalable Solution for High Energy Physics

Authors:

JUNE-WOO JUHN
Senior Researcher
NFRI

KANG JANGHEE
Chief Research Engineer
Durutronix

MATHIEU NAU
Sr. Signal Processing Engineer
Vadatech Asia-Pacific

CONSTANTIN BERNARD
Pre-Sales Engineer
Vadatech Asia-Pacific

Customer Application: High Density, High Speed Acquisition for Plasma Control KSTAR Tokamak

The National Fusion Research Institute (NFRI) of Korea, a world-renowned research institute, recognized the need to upgrade their plasma control system. In common with many of their counterparts in the high energy physics community, NFRI is adopting the MicroTCA.4 architecture as a common platform for high performance embedded computing.

The research team started with MicroTCA.4 as a reference platform for their high speed, high density data acquisition system and approached VadaTech with a list of specifications, including high speed and high density acquisition, with line rate data transfer to a Processor AMC (PrAMC).

"Electron density is a primary critical parameter in Tokamak plasma physics research. Interferometry is a diagnostic technique widely used for the measurement of electron density. There are a variety of interferometers, each system having a specific scheme for phase comparison.

NFRI & Durutronix are in the process of researching 'digital phase comparison' (Figure 2) instead of the traditional 'analog phase' (Figure 1) method using the VadaTech MicroTCA.4 hardware platform to measure electron densities in KSTAR Tokamak. We have identified the possibility throughout the preliminary experiment last year (Figure 3). We have a plan to perform more research to improve accuracy and reliability. The final goal is to analyze high accuracy electron density in real time at KSTAR Tokamak."

- June-Woo Juhn & Kang Janghee

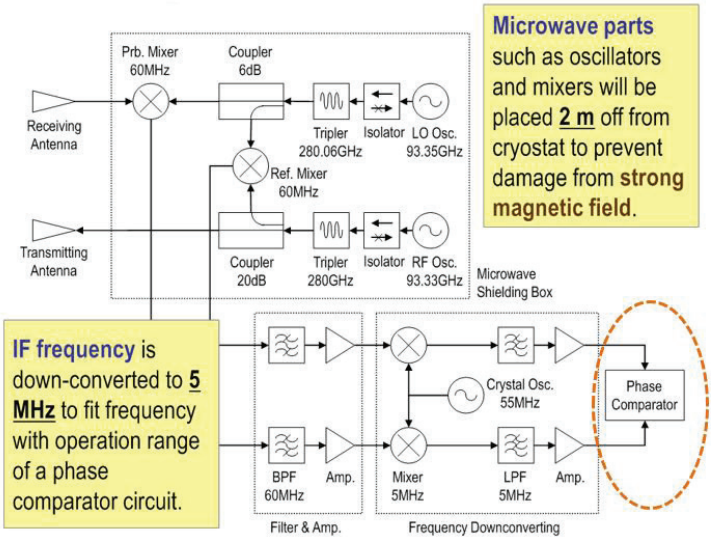

Figure 1: Schematic diagram of microwave system[1]

[1] Y. U. Nam (National Fusion Research Institute, KOREA) "Multi-fringe counting technique of millimeter-wave interferometer system for KSTAR"

After a careful analysis of MicroTCA.4 boundaries and selecting the appropriate Xilinx FPGA and analog-to-digital converter (ADC), VadaTech designed the AMC523 dual DAC module and MRT523 rear transition module for the MicroTCA.4 chassis. The system meets the requirements of the plasma control system while providing excess capacity for flexibility and future scalability.

Architecture Choice:

NFRI R&D experts collaborated with the ITER nuclear fusion research community and local technical support to finalize the architecture, balancing a complex set of parameters created by the high speed and high density specifications.

Channel Density Challenge:

The first challenge was to optimize the architecture to fit as many acquisition channels as possible, without compromising analog and digital signal integrity. VadaTech selected the AD9653 device from Analog Devices (quad, 16 bit, 125 MSPS ADC), and chose to dedicate the MRT523 rear transition module (MicroTCA .4 RTM) for the analog-to-digital conversion. This architecture gives the designer enough space to fit three AD9653 devices on the PrAMC to enable a total of 12 acquisition channels. This architecture keeps the analog signals in the RTM and they do not cross the backplane to the front card, thus providing the best isolation between the high speed digital signals, such as those from the FPGA and fabric, and the analog signals. Having the 12 analog inputs in the rear of the chassis also made it easier to integrate and cable the dense acquisition system in a cabinet on site.

Data Rate Challenge:

The second challenge was to handle the data rate of 24 Gb/s generated by the 12 ADC channels. VadaTech

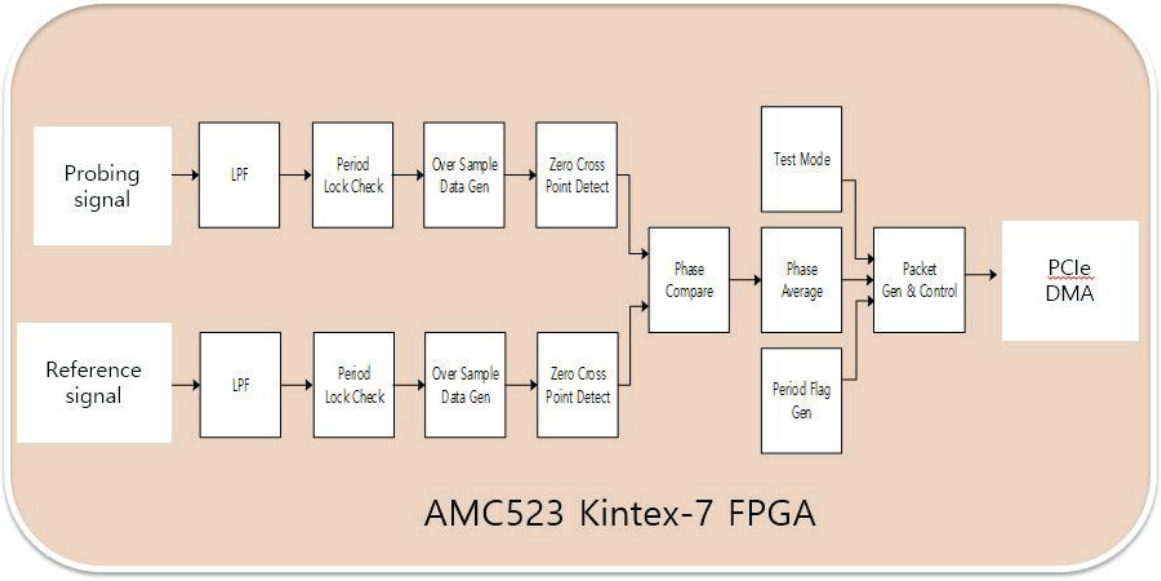

Figure 2: Digital phase comparison scheme at preliminary experiment

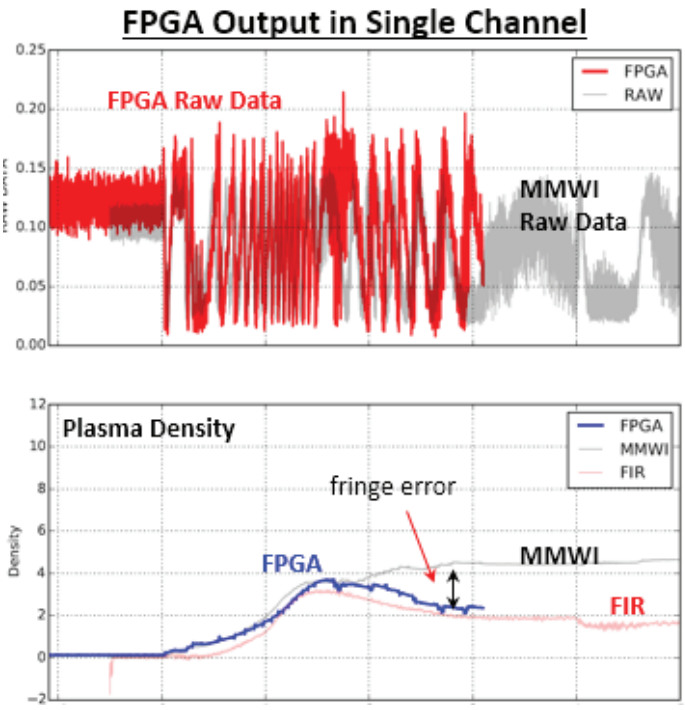

Figure 3: KSTAR preliminary experiment result

selected a Xilinx Kintex XC7K410T FPGA(406720 logic cells, 1540 DSP slices and 28620 Kb RAM blocks) in order to give NFRI enough processing power to implement its algorithms. The high speed buffering is handled by 2 GB of DDR3 memory, with enough bandwidth and capacity to do real time buffering of 600ms of acquisition.

To support the data transfer between the FPGA and the acquisition server, VadaTech provided the customer with different high speed paths:

1. For applications with an acquisition server running on a PrAMC, the system can use the fabric interface (lanes 4 to 11 of the backplane, up to PCIe 8x gen2). With a maximum data rate of 32 Gb/s, this path provides enough bandwidth to do real time acquisition.

2. For systems using an external acquisition server, VadaTech included 4 SFP+ connectors with a direct LVDS link to the FPGA's GTX blocks.

In addition, a dual Maxim MAX5878 DAC (16 bit, 250 MSPS) on the AMC523 is useful for applications using analog outputs, such as control loop, calibration and tests.

Physics experiments use their own high precision reference clock and trigger network. VadaTech designed a flexible clock and trigger routing on the AMC523, to cover every possible case (Figure 4).

The reference clock can either come from the on-board clock generator, the backplane (TCLKA, TCLKB, TCLKC or TCLKD), or the AMC523 front panel. Low jitter clocks are generated from the reference clock to drive the three quad ADC and the dual DAC. ADC and DAC sampling clocks can be adjusted by software, using the Silicon Labs Si5345A configuration tool.

The acquisition trigger can also come from the backplane (TCLKA, TCLKB, TCLKC or TCLKD) or from the AMC523 front panel.

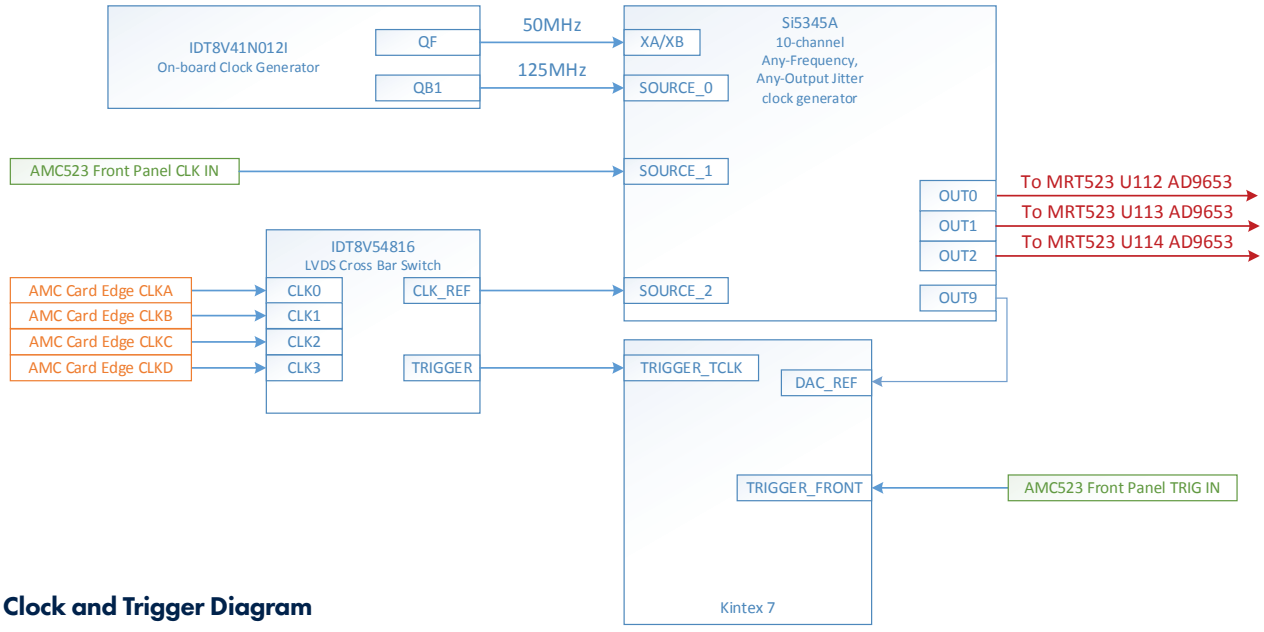

Figure 4: Clock and Trigger Diagram

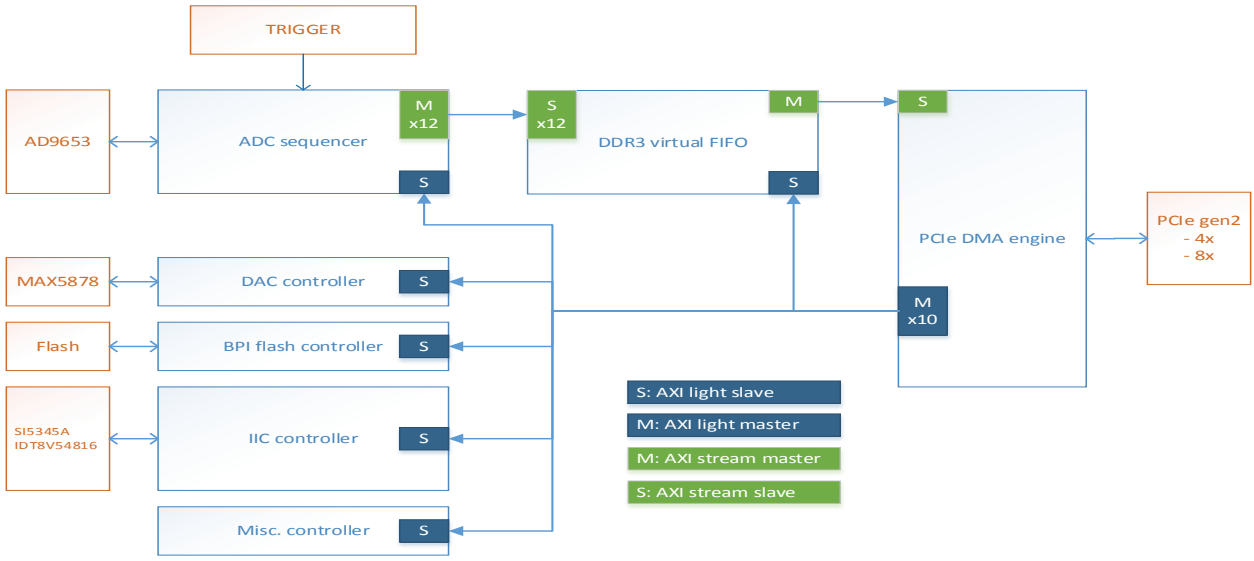

Figure 5: Acquisition IP Blocks

Software Integration Challenge:

With high density, high speed systems, the complexity of software development can become overwhelming. Designing acquisition software with a level of performance that best matches the capabilities of the hardware with the plasma control requirements involves a team of engineers with a wide range of specialties, including expertise in signal processing, FPGA design, networking, high-performance kernel drivers and more.

Most research institutes do not have sufficient in-house capability to provide expertise in all of these design disciplines. VadaTech's engineering team has extensive experience in complex system design, and in this application, the team put its expertise to work in alleviating the complexity of the hardware through a high level API. This allowed the end-user and local technical sales channel to concentrate on the development of EPICS drivers and allocate precious resources to their specific experiment tasks.

The first task on the road to this high level API was to design FPGA firmware that uses the full capability of the VadaTech MicroTCA .4 hardware.

The API is built around the AXI protocol (Figure 6), allowing a simple interconnection between VadaTech's firmware and the customer's own IP.

The DDR3 Virtual FIFO and the PCIe DMA engine are the main building blocks of the high speed interconnection between the FPGA and the acquisition server. The DDR3 Virtual FIFO allows the real-time buffering of 1 to 12 ADC channels. The PCIe DMA engine empties the Virtual FIFO at line rate (1.65 GB/s in PCIe 4x gen 2, 3.3 GB/s in PCIe 8x gen 2).

VadaTech engineers added an ADC sequencer to give the user flexibility in the definition of the acquisition sequence. Each ADC channel can be activated or deactivated. The acquisition mode can be one of the following:

- Single snapshot (start on trigger for a defined period of time)
- Repetitive snapshots (start on trigger for a defined period of time, stop acquisition for a defined period of time, start acquisition...)
- Free running (start on trigger for an unlimited period)

These three modes cover the requirements for most experiments. The association of an external reference clock and trigger, a cycle-accurate versatile sequencer and 64 bit samples' time-stamping make it possible to create complex experiments with an array of synchronous sensors with low jitter.

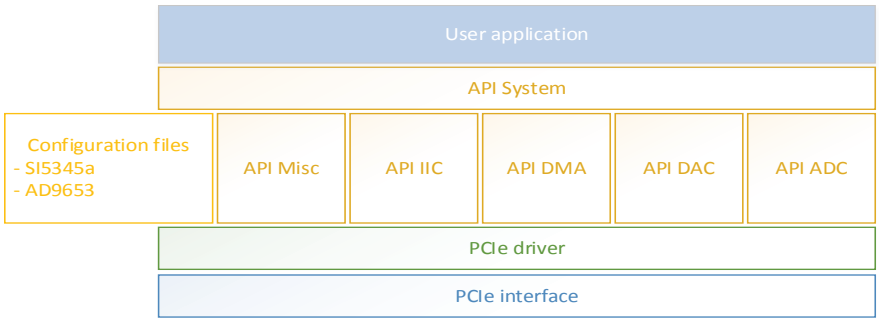

Figure 6: Layers providing easier control of the platform by the end-user

We designed a high level API to run on the server side.

This API is built with three layers, each layer with a decreasing level of complexity. This architecture gives users total control over the level of detail they need in their application. VadaTech engineers took care at each level to guarantee the lowest overhead possible.

VadaTech used its "Zero Copy" DMA IP with a fixed buffer allocation strategy for the PCIe driver in order to reduce the API overhead close to zero. The result is that the FPGAs write directly in the user application's buffers without any processing needed from the driver. The system API hides the complexity of this setup by providing a set of very high-level functions and example code.

This high performance design lets users focus on their own algorithms, and provides assurance that most of the server's CPU time is available for their own processing.

As this API is mainly designed for the scientific community, care was taken to assure compatibility with the main scientific Linux distribution, SL /MRGR. Scientific Linux and Real Time MRG (Red Hat) are both supported on the VadaTech AMC72X PrAMC series.

Security – High Density - Integration Choice

The VT812 chassis offers security with redundancy capabilities at both MCH and power module levels (Figure 7). This allows failover and hot-swap capability in case of failure.

Figure 7: Dual 500W/800W redundant power modules

Rear I/O connections provide secure cable management and easy access to instruments, improving the safety of the installation/maintenance team in a critical environment. The choice of SSMC connectors allows the 12 ADC and 2 DAC I/O to be available via the same rear panel (Figure 8).

The 2U VT812 chassis platform provides a hybrid of the MTCA.4 (4 slots) and MTCA.0 (4 slots) standards. This chassis solution enables the end-user to add a significant amount of storage. In some installations, the data acquisition function is linked to a separated storage rack accessible for analysis. This chassis allows the user to select between connecting to a distant storage rack and local storage in the chassis, accessible for off-line analysis.

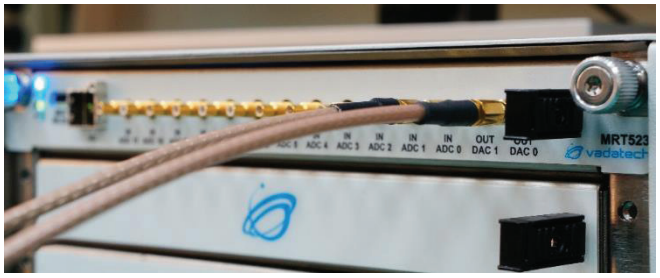

Figure 8: MRT523 SSMC connectors and SFP+ expansion

VadaTech manufactures six different chassis compatible with MTCA.4 specifications. For example, the VT816 1U chassis is an excellent choice for more compact acquisition platforms that don't require higher slot counts and redundancy. The chassis platform holds dual AMCs and the corresponding RTMs per the MTCA.4 specification. It has an integrated MCH, Intel Xeon E3 v2 processor and optional single/dual SSD drive for a complete integrated solution. See Figure 9 for an image of the VT816.

"Thanks to VadaTech's great technical support on the hardware and software platform, NFRI and Durutronix could focus on the design and implementation of the main algorithm and data analysis."

- June-Woo Juhn & Kang Janghee

With more than 300 products based on the open standard ATCA and MicroTCA architectures and a new DAQ_Series software package, VadaTech is providing access to technology to the researchers of the high energy physics community.

Figure 9: VT816, 1U µTCA.4 Chassis with 2 AMC Slots, PCIe Gen 3