AMC FPGA Carrier with FMC Interface

AMC513



OCTOBER 2010

KEY FEATURES

- AMC FPGA carrier for FPGA Mezzanine Card (FMC) per VITA-57
- AMC Ports 2-3 and 4-11 are routed to FPGA (protocols such as PCle, SRIO, XAUI, etc. are FPGA programmable)
- Xilinx Virtex-6 FPGA in FF1759 package
- AMC FCLKA, TCLKA, TCLKB, TCLKC and TCLKD are routed
- On board PLL for buffering/multiplying and jitter cleaner
- Option for up to 2GB of DDR-III memory
- · Option for QDR-II+
- Option for on board Freescale QorlQ PPC1020 with DDR-III
- RoHS compliant

The AMC513 is an AMC FPGA Carrier with an FMC (VITA 57) interface. The AMC513 is compliant to the AMC.1, AMC.2 and/or AMC.4 specification. The unit has an on-board, re-configurable FPGA which interfaces directly to the AMC Ports 2-3, 4-11, FCLKA, TCLKA, TCLKB, TCLKC, and TCLKD. The FPGA has an interface to the DDR-III memory (64-bit wide) and option for QDR-II+ (36 and 72-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The AMC513 has a single FMC connector per VITA-57. This allows having a single Carrier with multiple-different FMC modules in the system.

The on board PPC can run at 800MHz with 512 Mbytes of DDR-III, 8Mbytes of boot flash and 128MBytes of user Flash. The PPC has an x4 PCle interface to the FPGA in addition to it's local bus. The PPC has it's dual GbE routed to ports 0 and 1 of the AMC.

VadaTech can modify this product to meet special customer requirements without NRE (minimum order placement is required).



AMC FPGA Carrier with FMC Interface

SPECIFICATIONS

Architecture Physical Dimensions Single-width, Full-Height Width: 2.89 in. (73.5 mm) Depth: 7.11 in. (180.6 mm) Xilinx FGPA Virtex-6 Devices PLL multiplier/divider with jitter cleaner Single FMC slot DDR-III and QDR-II+ Standards AMC Type AMC.1, AMC.2, and AMC.4 (FPGA programmable) Module Management IPMI IPMI Version 2.0 PCIe Lanes x4 or x8 SRIO Lanes Dual x4 XAUI Lanes Dual port XAUI Aurora Lanes Dual x4 Ethernet GbE Dual 1000-BaseBX from PPC or FPGA			
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Configuration			
Power AMC513 Carrier is 40W without the Mezzanine			
Temperature Operating Temperature: 0° to 65° C (Air flow requirement is to be great	ater than 400 LFM)		
Storage Temperature: -40° to +90° C			
Environmental Vibration 1G, 5-500Hz each axis			
Shock 30Gs each axis	30Gs each axis		
Relative Humidity 5 to 95 percent, non-condensing			
Interface Connectors Front panel FMC			
Front Panel LEDs IPMI Management Control			
8 user defined LED			
Mechanical Hot Swap Ejector Handle			
Software Support Operating Systems Linux, Windows, Solaris and VxWorks			
Other			
MTBF MIL Handbook 217-F > TBD.	MIL Handbook 217-F > TBD.		
Certifications Designed to meet FCC, CE and UL certifications where applicable	Designed to meet FCC, CE and UL certifications where applicable		
Standards VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards		
Compliance RoHS and NEBS	RoHS and NEBS		
Warranty Two (2) years.	Two (2) years.		
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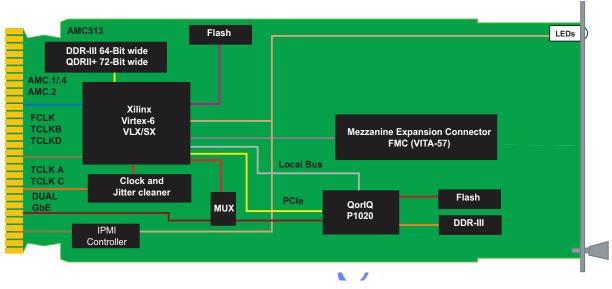
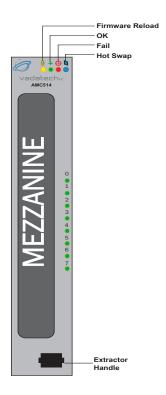


FIGURE 1. AMC513 Functional Block Diagram

FIGURE 2. AMC513 Front Panel



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ORDERING OPTIONS

AMC513 - ABC - DEF - GHJ			
A = DDR-III Memory	D = QorlQ CPU	G = PCle option	
0 = None 1 = 1Gbytes 2 = 2Gbytes	0 = None (FPGA is loaded via the Flash) 1 = Reserved 2 = Reserved 3 = Reserved 4 = 1020 @800MHz (FPGA is loaded by CPU	O = No PCle (ports 4-11) 1 = PCle on ports 4-7 2 = PCle on ports 8-11	
B = QDR-II+ Memory	E = FPGA	H = Operating Temp	
0 = None 1 = 2 x 36 (single chip) 2 = 2 x 72 (two chips) 3 = Reserved	1= Reserved 2= Reserved 3= Reserved 4= XC6VLX240T 5= XC6VLX365T 6= XC6VLX550T 7= XC6VSX475T 8 = Reserved	0 = Commercial 1 = Industrial	
C = Front Panel	F = FPGA SPEED	J = Conformal Coating	
1 = Reserved 2 = Mid-Height 3 = Full-Height	1 = Low 2 = High	0 = None 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic	





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