VME599

Quad ADC @ 3.2 GSPS or Dual ADC @ 6.4 GSPS, FPGA Kintex UltraScale



Key Features

- VME open standard form factor
- FPGA Xilinx UltraScale™ XCKU115
- ADC based on TI ADC12DJ3200
 - Quad 3.2 GSPS or Dual 6.4 GSPS
- Dual 1/10GbE to FPGA
- Dual bank of x64 DDR-4 and Single bank of x32 DDR-4 to FPGA
- Quad Core ARM CortexA53 at 1.6GHz per core
- GbE to ARM
- 4GB x32 DDR4 to ARM
- 14x LVCMOS and 34x LVDS to backplane P2

Benefits

- Sampling rate >6 GSPS for IF radar and EW applications
- Xilinx UltraScale™ XCKU115 FPGA provides powerful compute resource
- Flexible FPGA booting and module control via the I.MX8M Mini
- Electrical, mechanical, software, and system-level expertise in house
- AS9100 and ISO9001 certified company
- Full system supply from industry leader





VME599

The VME599 provides dual ADC sampling rates of up to @6.4GSPS at a 12-bit resolution TI ADC12DJ3200 or quad inputs at @3.2GSPS (or dual ADC12DJ2700 for two channels @5.4GSPS or four channels @2.7GSPS).

The unit has an onboard, re-configurable UltraScale+™ XCKU115 FPGA that directly interfaces with ADC and three banks of DDR4 memory channels. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host. The Dual 64-bit wide DDR-4 bank has total of 16 GByte and the single bank of 32-bit DDR-4 has 4GByte

The VME599 have on board wide-band PLL which provides the RF sampling clock to the ADC parts (both ADC receive the same sampling clock). This PLL can lock into an external clock routed from the front panel clock input.

The module has dual 1/10GbE to the FPGA (each port speed can be defined independently), both via RJ45 to the front panel. This allows digitized data to be transferred to external host.

The on-board quad core ARM processor provides flexibility to monitor and manage the FPGA. The CPU can load the FPGA image via PCIe. The onboard CPU monitors all the temperature sensors which can provide real time data to an external host. The CPU has 4GByte of memory as well and SDHC socket and a 64GByte of Flash to boot and store data.

The module takes power from P1 but does not implement VME bus transactions. Further from the FPGA there are 14 LVCMOS and 34 LVDS pairs that are routed to P2. VME599 use 160 pin connectors on the backplane.

This makes VME599 suitable for signal capture/analysis applications such as COMINT/SIGINT, radar, research and instrumentation.



Figure 1: VME599



Figure 2: VME599 without Heatsink



Figure 3: VME599 with Heatsink

Block Diagram

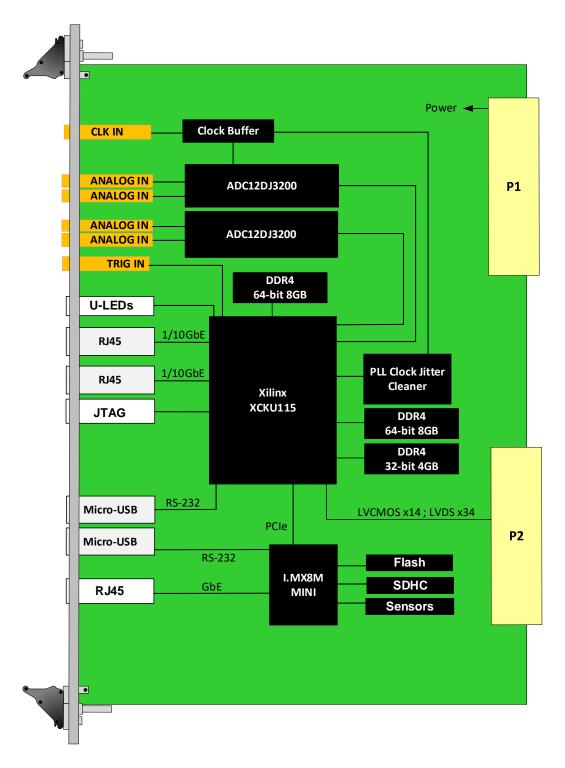


Figure 1: VME599 Block Diagram

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high-speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied precompiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

•			
Architecture			
Physical	Dimensions	Height: 6U	
		6.366 x 9.187 (PCB size)	
		Single slot	
Туре	VME FPGA ADC	Xilinx UltraScale™ XCKU115 FPGA	
		Three banks of DDR4 (dual 64-bit and single 32-bit)	
		Dual TI ADC	
		14xLVCMOS and 34x LVDS to P2	
Standards			
VME	Туре	VME SSTL 160 pins (P2 B not routed - no VME bus transaction)	
Configuration			
Power	VME599	Up to 120W (FPGA load and airflow dependent)	
Environmental	Temperature	See ordering option J	
		Storage Temperature: -40° to +85°C	
	Vibration	3-10 Hz displacement amplitude 1 mm; 10-50 Hz acceleration amplitude 0.2g	
		½ sine pulse, 15g, 20ms	
		5 to 95% non-condensing	
	•	Air-cooled; minimum required CFM applicable	
Front Panel	Interface Connectors	FPGA 2x1/10G via RJ-45, 1x JTAG, 1x Serial via the single USB on front panel	
		CPU 1x GbE via RJ-45, 1x Serial via the single USB on front panel	
		4x RF, CLK and Trigger Analog Input via SMA-F	
	=== *	User LEDs from FPGA and Status LEDs from CPU	
		Ejector Handle	
Software Support	Operating Systems	Agnostic	
Other			
MTBF	MIL Hand book 217-F@ TBD hrs		
Certifications	Designed to meet FCC, CE and UL certifications, where applicable; designed to meet UL-60950 where applicable; ESD design to standard specification, as applicable IEEE 1101.10.		
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards; VadaTech is RoHS Compliant; Fabricated to pass UL94V-0;		
Warranty	2 years per VadaTech T&Cs		

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as preconfigured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VME599 - A00-DE0-G0J

A = RF Direct Clock Sampling	D = ADC	G = Clock Holdover Stability
0 = Reserved 1 = Onboard Wideband PLL	0 = ADC12DJ3200 1 = ADC12DJ2700 (*) 2 = Reserved	0 = Reserved 1 = Stratum-3 (TCXO)
	E = FPGA Speed	
	1 = Reserved 2 = High 3 = Highest	
		J = Temperature Range and Coating
		0 = Commercial (-5° to +55°C), No coating 1 = Commercial (-5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (-5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (-20° to +70°C), No coating 4 = Industrial (-20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (-20° to +70°C), Humiseal 1B31 Acrylic

^{*} Conditions may apply - Contact VadaTech Sales

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Related Products

VME215



- Managed Layer 2 and layer 3 switch
- 12 ports of 10/100/1000 via RJ-45 on the base board
- 12 ports via SFP (daughter module)

AMC599



- Xilinx UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS or quad ADC @ 3.2 GSPS with TI ADC12DJ3200
- Option for ADC12DJ3200 or ADC12DJ2700

VPX599A



- 3U FPGA Dual ADC and Dual DAC per VITA 46
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Health Management through dedicated Processor

Contact

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