VPX592

FPGA/FMC Carrier, Kintex UltraScale™, 3U VPX

VPX592

Key Features

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner
- VHDL reference design with source code
- Protocols such as PCIe, SRIO, 10GbE/40GbE, etc. are FPGA programmable
- Compatible with VadaTech and 3rd party FMCs
- 20 GB of DDR4 Memory (2 banks of 64-bit wide, and single bank of 32-bit wide)
- Health Management through dedicated Processor

Benefits

- XCKU115 FPGA provides 5,520 DSP slices for complex processing
- 20 GB of DDR4 memory for fast local data buffering
- Reference design with VHDL source code speeds application development
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX592

The VPX592 is a FPGA Carrier (VITA 46) with an FMC (VITA 57) interface. The unit has an onboard, re-configurable Xilinx Kintex UltraScale™ XCKU115 FPGA which has 5520 DSP Slices. The FPGA interfaces directly to the FMC DP0-9 and all FMC LA/HA/HB pairs.

The VPX592 routes high-speed serial links directly from the FPGA to backplane, allowing the core to interface directly to the host with protocols such as 40GbE, 10GbE, PCIe or SRIO. The FPGA has 2 banks of 64-bit and single bank of 32-bit wide DDR4 memory (20 GB total). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The module supports dual GbE and, dependent on FPGA code loaded, PCIe up to Gen3 (dual x4 or x8 lane), or dual SRIO, 10GbE or 40GbE on P1. There are dual x4 lanes routed to P2 for direct FPGA-to-FPGA connection using lightweight protocols such as Aurora (backplane dependent) and additional 16 LVDS pairs are routed to P2.

The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

Please contact VadaTech for details of Conduction Cooled versions.

Figure 1: VPX592

Block Diagram

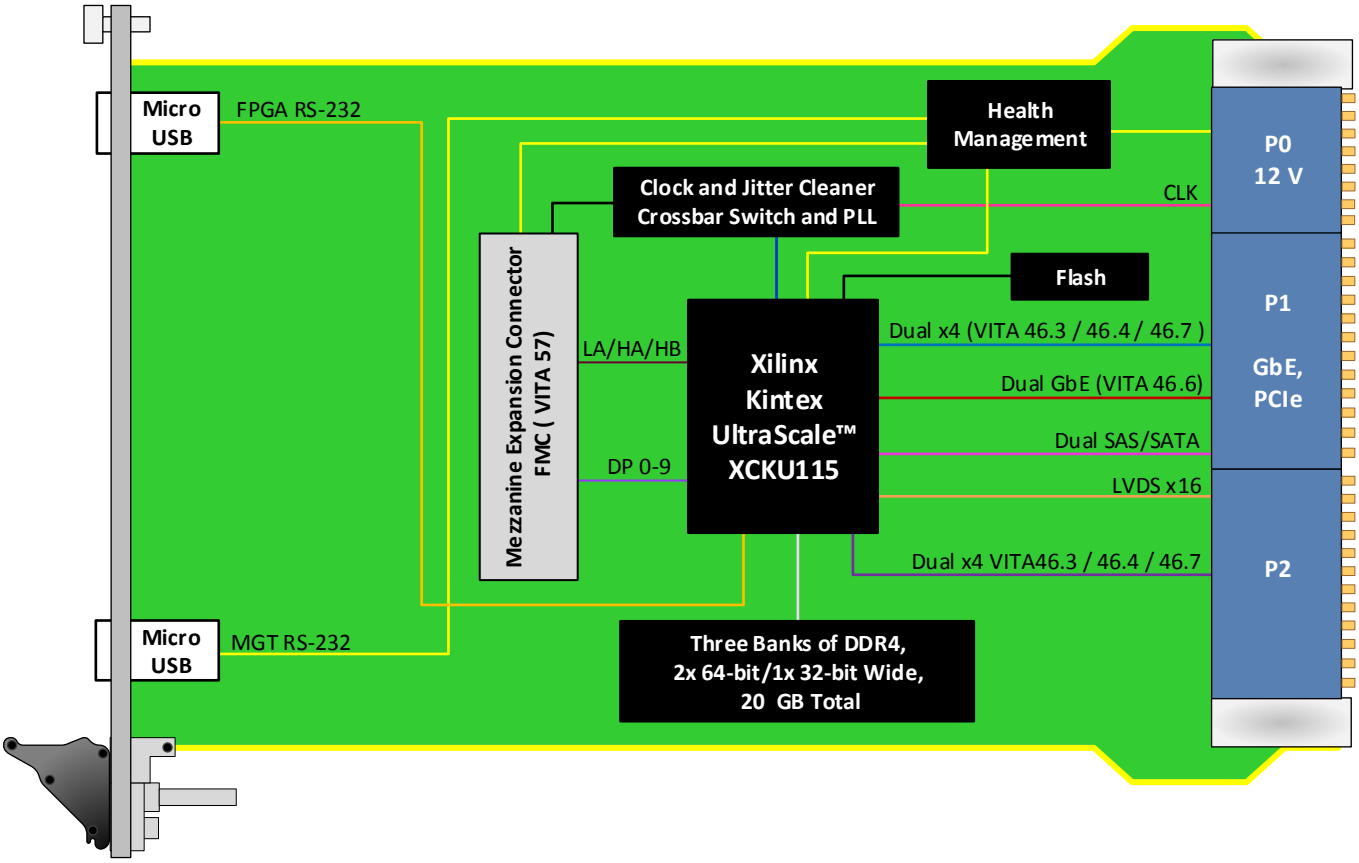

Figure 2: VPX592 Functional Block Diagram

Front Panel

Figure 3: VPX592 Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
FPGA		Xilinx Kintex UltraScale™ XCKU115
Configuration		
Power	**VPX592**	~TBD W (dependent on FPGA load)
Memory		Two banks of DDR4, 64-bit wide and single bank of 32-bit wide DDR4 (20 GB total)
Front Panel	**FMC**	Single FMC slot
	Micro USB	RS-232 from Health Management CPU and RS-232 from FPGA
	LEDs	User defined by the FPGA and Health Management
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	Dual x4 fabric on P1 (PCIe Gen3/10GbE/40GbE/SRIO per FPGA load)
		Dual GbE on P1
		Dual x4 fabric on P2 (optional) with 16 LVDS
	Power Supplies	On P0: VS1 = 12V
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX592 – 0BC-DEF-GHJ

	D = FPGA Speed	G = Applicable Slot Profiles
	1 = Reserved 2 = High 3 = Highest	0 = 5 HP
B = Expansion Plane (P2)	**E = Clock Holdover Stability**	**H = Environmental**
0 = Not routed 1 = Routed	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification
C = VPX Connector Type	**F = PCIe Option (P1) for Data Port 1/2**	**J = Conformal Coating**
0 = Standard 50u Gold Rugged 1 = KVPX Connectors	0 = No PCIe 1 = PCIe/None 2 = None/PCIe 3 = PCIe/PCIe	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

AMC592

- AMC FPGA carrier for FMC per VITA 57
- Xilinx UltraScale™ XCKU115 FPGA
- Supported by DAQ Series™ data acquisition software

FMC108

- FPGA Mezzanine Card (FMC) per VITA 57
- Two QSPF+ cages for 10GbE/SRIO/PCIE and Aurora
- Re-driver on both ports for a better signal quality

FMC228

- FPGA Mezzanine Card (FMC) per VITA 57
- Quad ADC based on AD9234
- Option for Direct RF sampling clock via front panel

Contact

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