VPX994

6U VPX I/O Module with six QSFP+ ports



Key Features

- 6U VPX Module with six QSFP+
- Clock Data Recovery (CDR) per lane
- Data rates from 1.25 to 10.3125 Gb/s are programmable per port (i.e. 2.5, 3.125 Gb/s etc.)
- Adaptive Equalization up to 34-dB
- Adjustable Transmit from 600 to 1300 mVp-p
- Adjustable Transit De-emphasis to -15dB
- Front panel jacks to measure the +12V and +3.3VAUX

Benefits

- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company





VPX994

The VPX994 is a 6U VPX module with 6 QSFP+ transceivers. The module has a CDR per port for better signal integrity. Each CDR is tunable individually for different speed. The module is protocol agnostic.

There are 12 ports that come from the P1 connector to the first three QSFP+. From each P2/P3/P4 ports 0/4/8/12 are routed to each of the QSFP+ transceivers.

The front I/O allows access to the NVMRO, *SYSRESET and DISCRETE1 signal.

Front panel Jacks allows measuring the +12V and +3.3V_AUX. The Module also has Jacks to Chassis Ground as well as the Digital Ground.

The module has one LED per CDR Lock port.



Figure 1: VPX994



Figure 2: VPX994 Front View



Figure 3: VPX994 No Flash



Figure 4: VPX994 Top View

Block Diagram

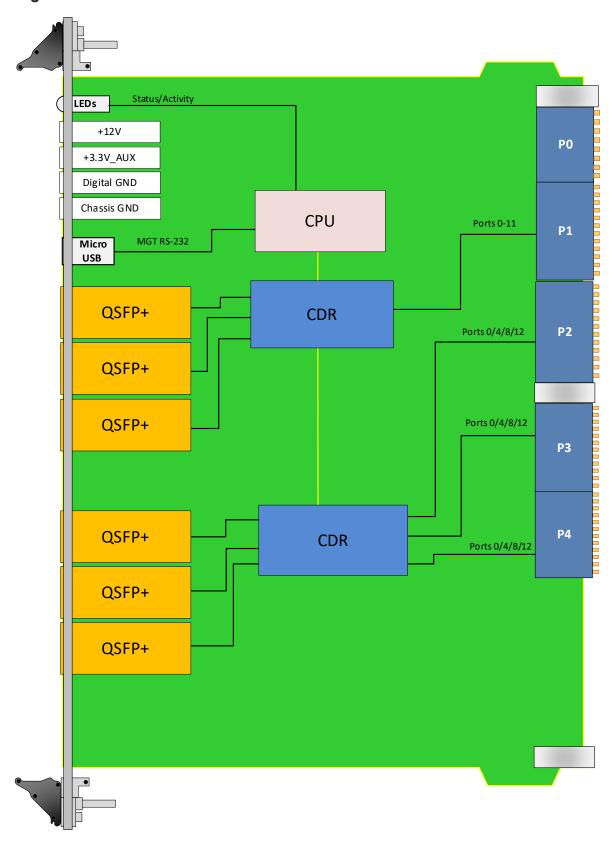


Figure 5: VPX994 Functional Block Diagram

Pinout Block Diagram

						1		4		l		1	
	1	h ×		1	× 4			1	ъ ×				
	2			2				2				2	SERI ×
	3			3				3			3	SERDES ×4	
	4			4				4			4		
	5	ъ ×		5	⊢×			5	ъ ×			5	
	6			6]		6				6	SER ×
	7			7			P2_	7			7	SERDES ×4	
	8			8				8			P1_	8	
	9	1 ×	1	9	⊢×]		9	1 ×	1		9	SERDES ×4
	10			10]		10				10	
	11			11				11				11	
P4_	12		23	12				12				12	
	13	1 ×		13	ъ×			13	ъ×			13	
	14			14				14				14	
	15			15				15			15		
	16			16			16			16			
	Ro w G			Ro w G				Ro w G				Row G	

Figure 6: VPX994 P1/P2/P3/P4 SERDES

Specifications

Architecture						
Physical	Dimensions	6U, 1" pitch				
Туре	I/O	Six QSFP+ Ports				
Configuration						
Power	VPX994	15W				
Front Panel	Interface Connectors	QSFP+				
	Micro USB	RS-232 from on board CPU				
		NVMRO, *SYSRESET and DISCRETE1 front I/O access				
		Jacks to +12V, +3.3V_AUX, Chassis Ground and Digital Ground				
LEDs		CDR Lock LED per port				
VPX Interfaces	Slot Profiles	See Ordering Options				
Rear IO		P0: NVMRO, SYSRESET				
		P1: First 12 ports to QSFP+				
		P2/P3/P4 ports 0/4/8/12 routed to the QSFP+				
Software Support	Operating System	Agnostic				
Other						
MTBF	MIL Hand book 217-F@ TBD hrs					
Certifications	Designed to meet FCC, CE and UL certifications, where applicable					
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards					
Warranty	Two (2) years, see Vada	aTech Terms and Conditions				

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as preconfigured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX994 - A0C-D00-GHJ

A = QSFP+ Transceiver	D = VPX P2 Connector	G = Applicable Slot Profiles		
0 = None 1 = 40Gb (SR) 2 = 40Gb WDM (SR) 3 = 40Gb (LR) 4 = Reserved 5 = Reserved	0 = Loaded 1 = Not Loaded 2 = P2A loaded (no P2B) 3 = Reserved	0 = 5 HP, VITA 48.1		
		H = Environmental		
		See Environmental Specification		
C = VPX Connector Type		J = Conformal Coating		
0 = Standard 50u Gold Rugged 1 = KVPX Connectors		0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic		

Environmental Specification

	Air Cooled		Conduction Cooled			
Option H	H = 0	H = 1	H = 2	H = 3	H = 4	
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)	
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)	
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)	
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)	
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products



- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner



- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

Contact

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