AMC591

ADC @ 56 GSPS, 2 or 4 Channel, UltraScale, AMC

AMC591

Key Features

- Double module, mid-size or full-size
- Xilinx UltraScale™ XCVU190 FPGA
- ADC 8-bit @ up to dual 56 GSPS
- 2 x 56 or 4 x 28 GSPS channels
- ADC is 65 nm CMOS process technology
- 16 GB of DDR4 Memory (2 banks of 64-bit)
- Very low power consumption (5W for the ADC)
- Calibration warning and over-range flags
- –3 dB analog input bandwidth nominally 15 GHz
- Internal 14 GHz VCO/PLL per I/Q ADC pair
- Differential analog input: 1.0V PPD
- Tongue 2 for additional SERDES

Benefits

- Highest sampling rate for the module size in the industry
- Uses MB8AC2070 ADC
- Low power consumption – CMOS process technology
- Flexible selection of sample rate and channel count
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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AMC591

The AMC591 used the Fujitsu MB8AC2070 Analog to Digital Converter (ADC) to provide dual 56 GSPS or quad 28 GSPS from four channels ADC (user selectable). The board is compliant to AMC.0 specifications.

The AMC591 allows the implementation of extremely fast, high-resolution ADCs in CMOS process technology. The ADC is ideal for applications that require ultra-high-performance analog and digital processing such as 100G applications. Achieved input bandwidth depends on system configuration and operating conditions, contact VadaTech for details.

The AMC591 has a Xilinx UltraScale™ XCVU190 FPGA which has 1800 DSP Slices. The FPGA interfaces directly to the AMC connectors over both tongue 1 and tongue 2, supporting up to 22 lanes routed to GTY transceivers for board-to-board connectivity (chassis dependent). The FPGA has 2 banks of 64-bit DDR4 memory (16 GB total).

The tongue 2 connections can also provide dedicated lanes to communicate with high speed processors such as VadaTech AMC750/AMC751. Chassis such as the VadaTech VT884/VT815 can accept modules with Tongue two connector.

The Module has two routing options for high speed SERDES from the FPGA to the backplane:

- Option B = 0 most of the SERDES are routed to Tongue 2 (Figure 2)
- Option B = 1 most of the SERDES are routed to Tongue 1 (Figure 3)

This allows the module to provide the most flexibility depending on the chassis routing.

Figure 1: AMC591

Block Diagram

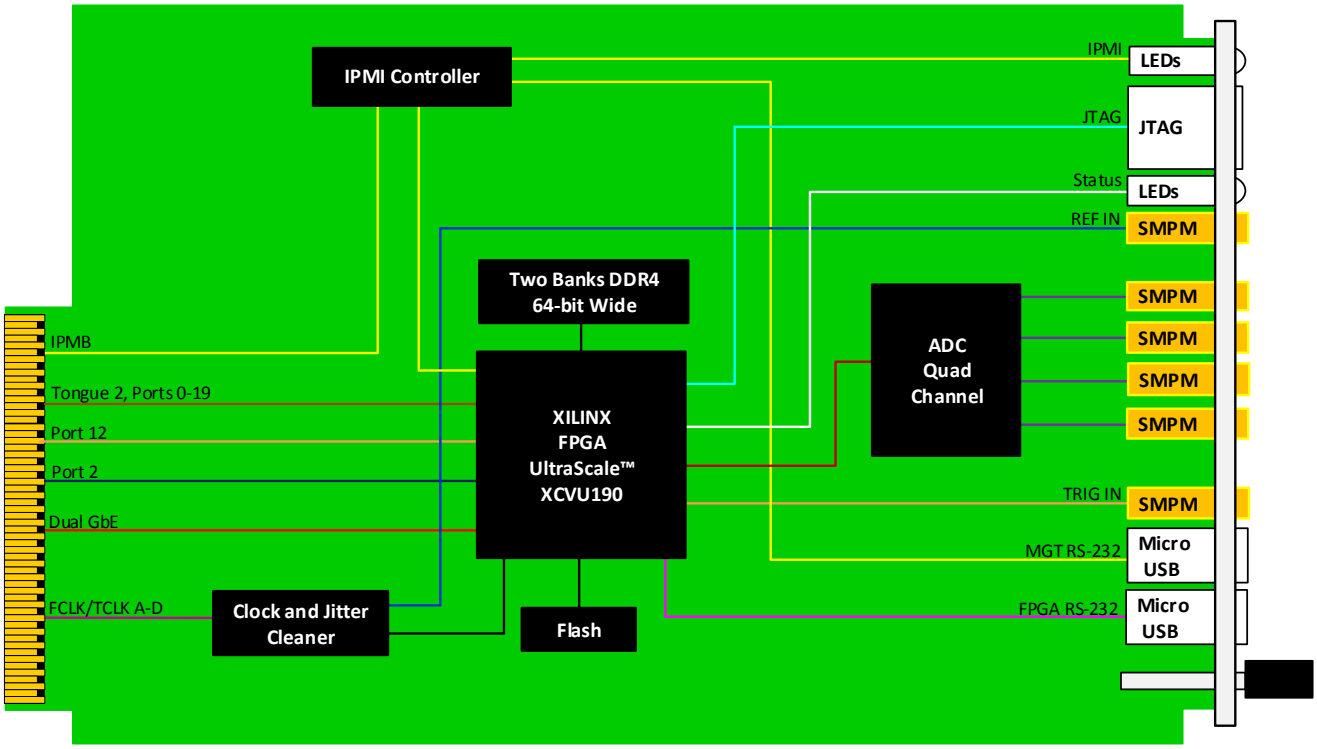

Figure 2: AMC591 Functional Block Diagram (Option B = 0)

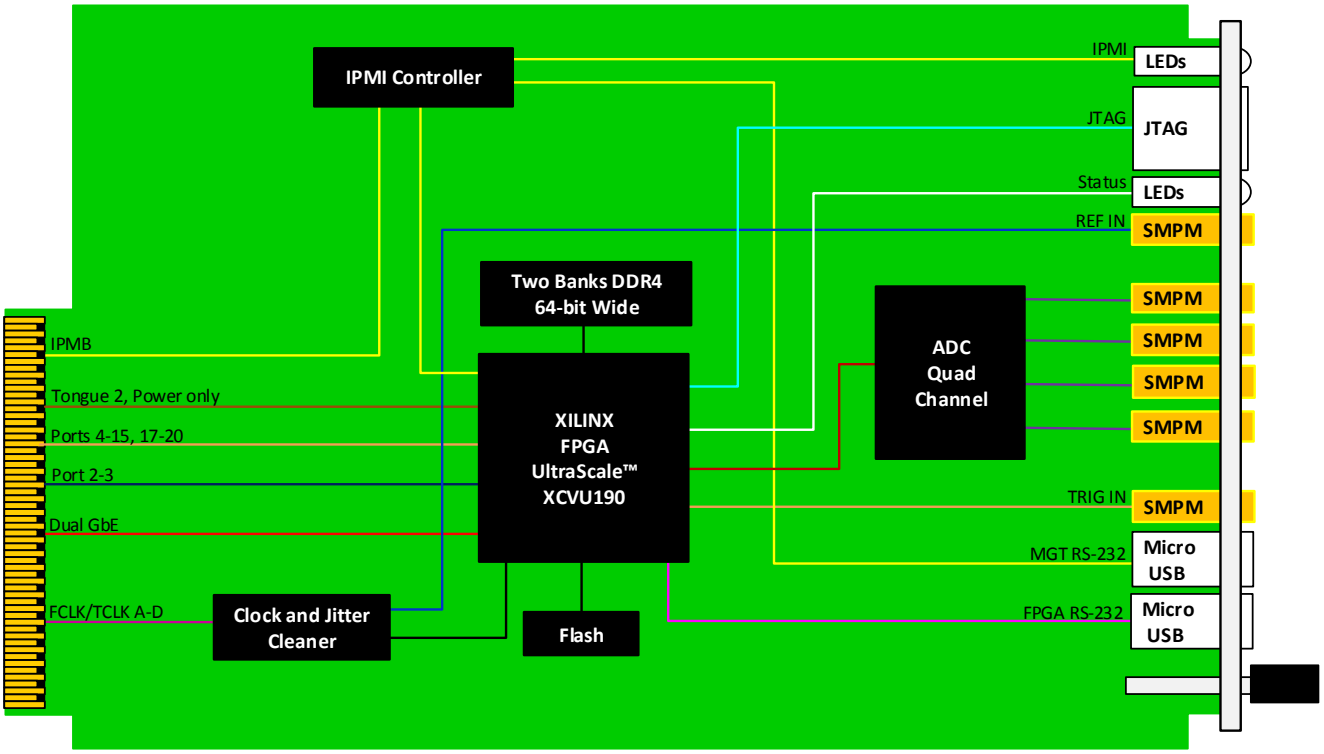

Figure 3: AMC591 Functional Block Diagram (Option B = 1)

Front Panel

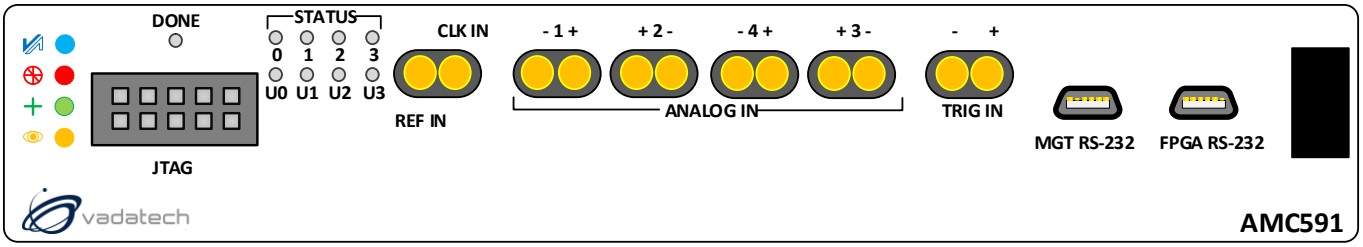

Figure 4: AMC591 Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	Double module, mid-size with full-size option
		Width 5.85” (148.5 mm)
		Depth 7.11” (180.6 mm)
Type	**AMC ADC**	ADC, up to 4 input channels, quad 28 GSPS or dual 56 GSPS
Standards		
AMC	**Type**	AMC.0
Module Management	**IPMI**	IPMI v2.0
Configuration		
Power	**AMC591**	90W (application specific)
Environmental	**Temperature**	See Ordering Options and Environmental Spec Sheet
		Storage Temperature: –40° to +85°C
	Vibration	1G, 5-500 Hz on each axis
	Shock	30Gs each axis
	Relative Humidity	5 to 95% non-condensing
Electrical	**DNL/INL**	+/- 0.5 LSB, +/- 1.0 LSB
	SNDR	40 dBFS @ Fin = 1 GHz, 36 dBFS @ Fin = 17 GHz
	Output Rate	128 samples x 8-bit @ 437.5 MHz
	Signals	<100 fs rms jitter, <500 fs I/Q sample time error
Front Panel	**Interface Connectors**	SMPM as differential input for each channel
		SMPM Trig in
		SMPM Clock/Ref input
		IPMI and FPGA RS-232 via Micro USB
		FPGA JTAG
	LEDs	IPMI and Debug (user defined)
	Mechanical	Hot-swap ejector handle
Software Support	**Operating Systems**	Independent
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

AMC591 – ABC-000-00J

A = RF Direct Clock Synthesis		
0 = Front Panel 1 = Onboard Wideband PLL		
B = High Speed Lanes		
0 = Tongue 2 (See Figure 2) 1 = Extended (See Figure 3)		
C = Front Panel Size		**J = Temperature Range and Coating**
1 = Reserved 2 = Mid-size 3 = Full-size 4 = Extended (8 HP) 5 = Mid-size, MTCA.1 (captive screw) 6 = Full-size, MTCA.1 (captive screw)		0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Related Products

AMC104

- AMC PCIe Gen 3 carrier (x4 or x8)
- Double module, full-size
- Accepts any standard PCIe edge style module (connector is x16)

AMC750

- Processor AMC Intel® Xeon E5-2648L v4
- PCIe Gen 3 on Ports 4-7 and 8-11(AMC.1)
- x16 PCIe Gen 3 via Tongue 2, optional PCIe to Ports 12-15, 17-20

VT815

- MTCA Chassis Platform with rear I/O
- 19” x 9U x 14.9” deep (with handles 16.23” deep)
- Full redundancy with dual MicroTCA Carrier Hubs (MCH), dual cooling units and 3 PSUs

Contact

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DOC NO. 4FM737-12 REV 01 | VERSION 1.6 – OCT/19