AMC592

Kintex UltraScale FPGA Carrier for FMC, AMC



Key Features

- Single module, mid-size AMC (full-size optional)
- AMC FPGA carrier for FMC per VITA 57
- Xilinx UltraScale™ XCKU115 FPGA
- Supported by DAQ Series[™] data acquisition software
- AMC Ports 12-15 and 17-20 are routed to the FPGA for direct FPGA to FPGA board communication
- AMC Ports 4-11 are routed to FPGA per AMC.1, AMC.2 and AMC.4 (protocols such as PCIe, SRIO, 1/10/40GbE, etc. are FPGA programmable)
- Two banks of 64-bit wide and a single bank of 32-bit wide DDR4 for a total of 20 GB
- AMC FCLKA, TCLKA, TCLKB, TCLKC and TCLKD are routed

Benefits

- 20 GB of DDR4 memory
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company





AMC592

The AMC592 is an AMC FPGA Carrier with an FMC (VITA 57) interface. The unit has an onboard, re-configurable Kintex UltraScale FPGA which interfaces directly to the AMC FCLKA, TCLKA-D, FMC DP0-9 and all FMC LA/HA/HB pairs. The FPGA also has interface to three banks of DDR4 memory channels. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The AMC592 is compliant to the AMC.1, AMC.2 and/or AMC.4 specification, and supports direct AMC-to-AMC connections over Ports 12-15 and 17-20.

The AMC592 has a single FMC connector to accept FMCs from VadaTech's extensive range of data acquisition, networking and RF units, and other 3rd party VITA 57 compliant modules.

This VadaTech Product is suitable for <u>ASIC Emulation</u>. Also, see <u>Solution Brief</u> for an overview of a 56 GSPS digitizer with IRIGB/GPS timestamping.



Figure 1: AMC592

Block Diagram

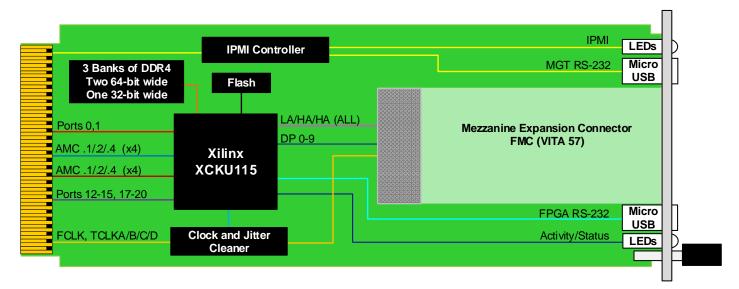


Figure 2: AMC592 Functional Block Diagram

Front Panel

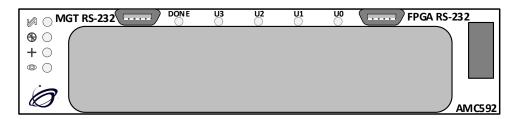


Figure 3: AMC592 Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied precompiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Data Acquisition

VadaTech offers a wide range of FPGA AMCs, RTMs, FMC Carriers and FMCs that can be combined to build a Data Acquisition (DAQ) sub-system. The DAQ Series software, when used with a supported hardware configuration, provides all that is needed to configure the system, acquire data and transfer it to a host processor. It also includes a user-configurable Graphical User Interface (Figure 4), which incorporates real-time display of acquired data. The host can be within the MTCA system or, via PCI113 or PCI123, in a separate PC. Full documentation is provided to allow users to customize system behavior or develop their own application on the AMC/FMC hardware.

The DAQ includes data acquisition software that allows users to get up and running quickly and easily, while providing a high level of performance and allowing the user to extend functionality by adding their own FPGA code. Please contact VadaTech sales for the latest information on supported combinations of VadaTech hardware. (Note that the DAQ Series software is not currently supported for 3rd party hardware).

Components provided in the DAQ software include:

- System libraries to configure clocking and triggers
- Sequencer to configure the acquisition (duration, start, stop)
- High-performance DMA firmware for acquiring ADC outputs and transferring to host processor
- Linux driver for host processor (e.g. AMC72x)
- EPICS channel access client API
- Pre-configured GUI (based on Qt Creator)

This software set allows the user to acquire, transfer and display data without the need for any user programming of the hardware. Status information is included in the GUI display, to ease integration and debugging activity.

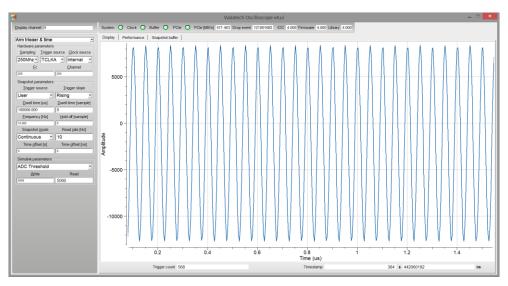


Figure 4: Typical Graphic User Interface Display

The data acquisition software provided as part of the DAQ can be used as-delivered without the user needing to develop any FPGA code.

Full source code is provided for the libraries, sequencer, DMA, Linux driver and GUI, allowing users to easily customize or brand to their own requirements at the exception of a low level PCIe IP from Xilinx provided only as Netlist (this low-level block doesn't require modification/customization from integrators or end-users).

Specifications

| Architecture | | | |
|-------------------|--|---|--|
| Physical | Dimensions | Single module, mid-size (full-size optional) | |
| - | | Width: 2.89" (73.5 mm) | |
| | | Depth 7.11" (180.6 mm) | |
| Туре | AMC FPGA Carrier | Xilinx UltraScale™ XCKU115 FPGA | |
| Standards | | | |
| AMC | Туре | AMC.1, AMC.2 and AMC.4 (FPGA programmable) | |
| Module Management | IPMI | IPMI v2.0 | |
| PCle | Lanes | Dual x4 via FPGA to AMC | |
| SRIO/Aurora | Lanes | Dual x4 via FPGA to AMC | |
| Ethernet | 10GbE and GbE | Dual GbE and 10/40GbE | |
| Configuration | | | |
| Power | AMC592 | Carrier is ~45W (without mezzanine) application specific (may go up to 65W) | |
| Environmental | Temperature | See Ordering Options and Environmental Spec Sheet | |
| | | Storage Temperature: –40° to +85°C | |
| | Vibration | Operating 9.8 m/s ² (1G), 5 to 500 Hz | |
| | | 30Gs on each axis | |
| | • | 5 to 95% non-condensing | |
| Front Panel | Interface Connectors | · | |
| | | Dual Micro USB for MGT RS-232, FPGA-RS-232 | |
| | LEDs | IPMI Management Control | |
| | | 4 user defined LEDs, 5 general status LEDs | |
| | | Hot-swap ejector handle | |
| Software Support | Operating System | None | |
| Other | | | |
| MTBF | MIL Hand book 217-F@ TBD hrs | | |
| Certifications | Designed to meet FCC, CE and UL certifications, where applicable | | |
| Standards | VadaTech is certified to both the ISO9001:2015 and AS9100D standards | | |
| Warranty | Two (2) years, see <u>VadaTech Terms and Conditions</u> | | |

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as preconfigured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

AMC592 - 0BC-DEF-GHJ

| | D = Ports 12-15 and 17-20 | G = Clock Holdover Stability |
|---|--|--|
| | 0 = Not connected to FPGA 1 = Connected to FPGA | 0 = Standard (XO) 1 = Stratum-3 (TCXO) |
| B = Trigger Routing | E = FPGA Speed | H = Temperature Range |
| 0 = All clocks to FPGA via Quad PLL 1 = Trigger clocks bypass Quad PLL | 1 = Reserved 2 = High 3 = Highest | 0 = Commercial (-5° to +55°C) 1 = Industrial (-20° to +70°C) 2 = Extended (-40° to +85°C)* |
| C = Front Panel | F = PCle Option | J = Conformal Coating |
| 1 = Reserved 2 = Mid-size 3 = Full-size 4 = Extended (8 HP) 5 = Mid-size, MTCA.1 (captive screw) 6 = Full-size, MTCA.1 (captive screw) | 0 = No PCle 1 = PCle on Ports 4-7 2 = PCle on Ports 8-11 3 = PCle on Ports 4-11 | 0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic |

Notes:

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Related Products

VT899



- MTCA System Platform 5" x 7U x 9" deep. (with handles 10" deep)
- Up to six AMCs: 6 full-size single-width or 3 full-size double width
- Redundant Cooling Units

FMC223



- FPGA Mezzanine Card (FMC) per VITA 57
- Single module AD9739 DAC 14-bit @ 2.5 GSPS
- 2 Vpp differential Analog output swing

UTC020



- Single module, full-size per AMC.0
- Dual -36V DC to -75V DC input, 936W (available in 468W)
- Hot-swappable with support for power module redundancy

^{*}Conduction cooled; temperature is at edge of module. Consult factory for availability.

Contact

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- · Mutual success

We deliver complexity

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- · Agile production
- · Accelerated deployment
- AS9100 accredited





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