# VPX551

## Dual Kintex UltraScale™, 6U VPX

VPX551

## Key Features

- Dual Kintex UltraScale™ XCKU115
- 16 GB of 64-bit wide DDR4 Memory to each FPGA
- Rear fibre I/O via VITA 66.5
- Front fibre via SFP+
- Health Management through dedicated Processor

## Benefits

- Each XCKU115 FPGA provides 5,520 DSP slices for complex processing
- Reference design with VHDL source code speeds application development
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™


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# VPX551

The VPX551 provides dual Kintex UltraScale™ XCKU115 FPGAs which interface directly to rear I/O via SERDES, LVDS and fiber. Each FPGA is supported by 16 GB of 64-bit wide DDR4 (2 x Bank of 8 GB) and 1 GB flash. Rear panel fiber I/O is via six VITA 66.5 x12 modules, each of which can be populated as transmit or receive. The front panel fiber I/O is via SFP+. The two FPGAs are connected by four SERDES lanes for high-speed communication.

The VPX551 includes platform health management/monitoring capability using VadaTech's field-proven IPMI software. An onboard management controller has the ability to access board sensors and manage FPGA image updates.

The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

Please contact VadaTech for details of Conduction Cooled versions.

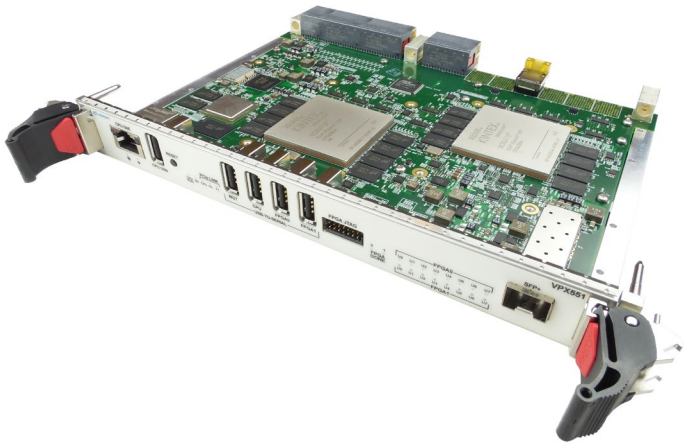

Figure 1: VPX551

# Block Diagram

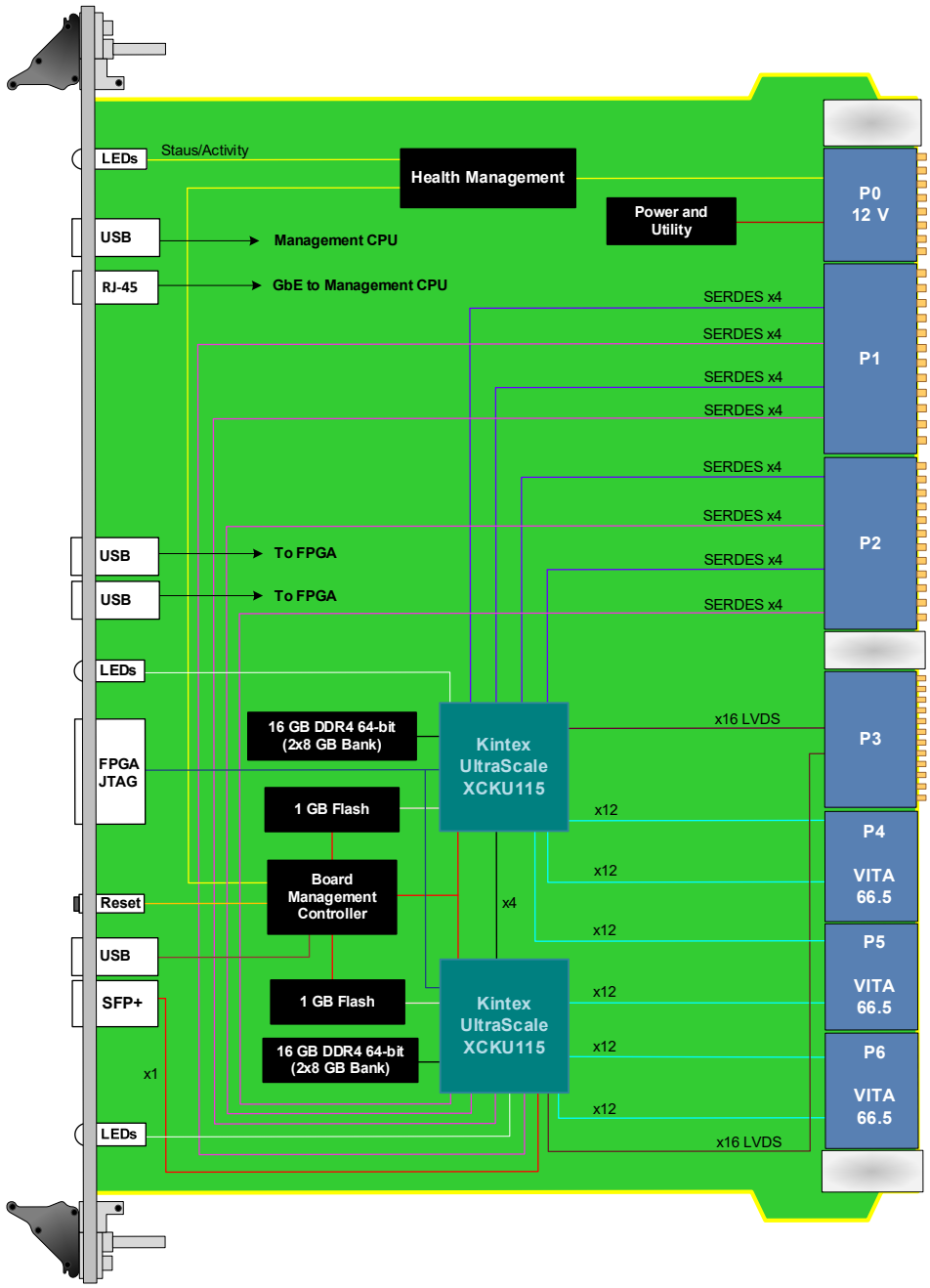


*Figure 2: VPX551 Functional Block Diagram*

# Front Panel

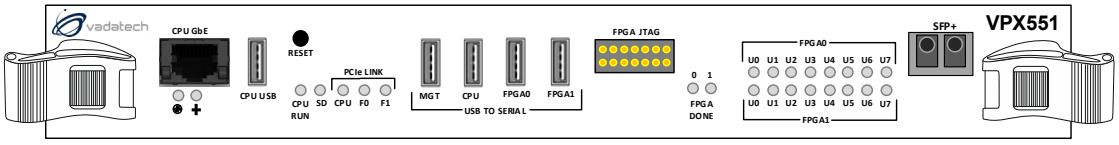


*Figure 3: VPX551 Front Panel*

# Backplane Pinout

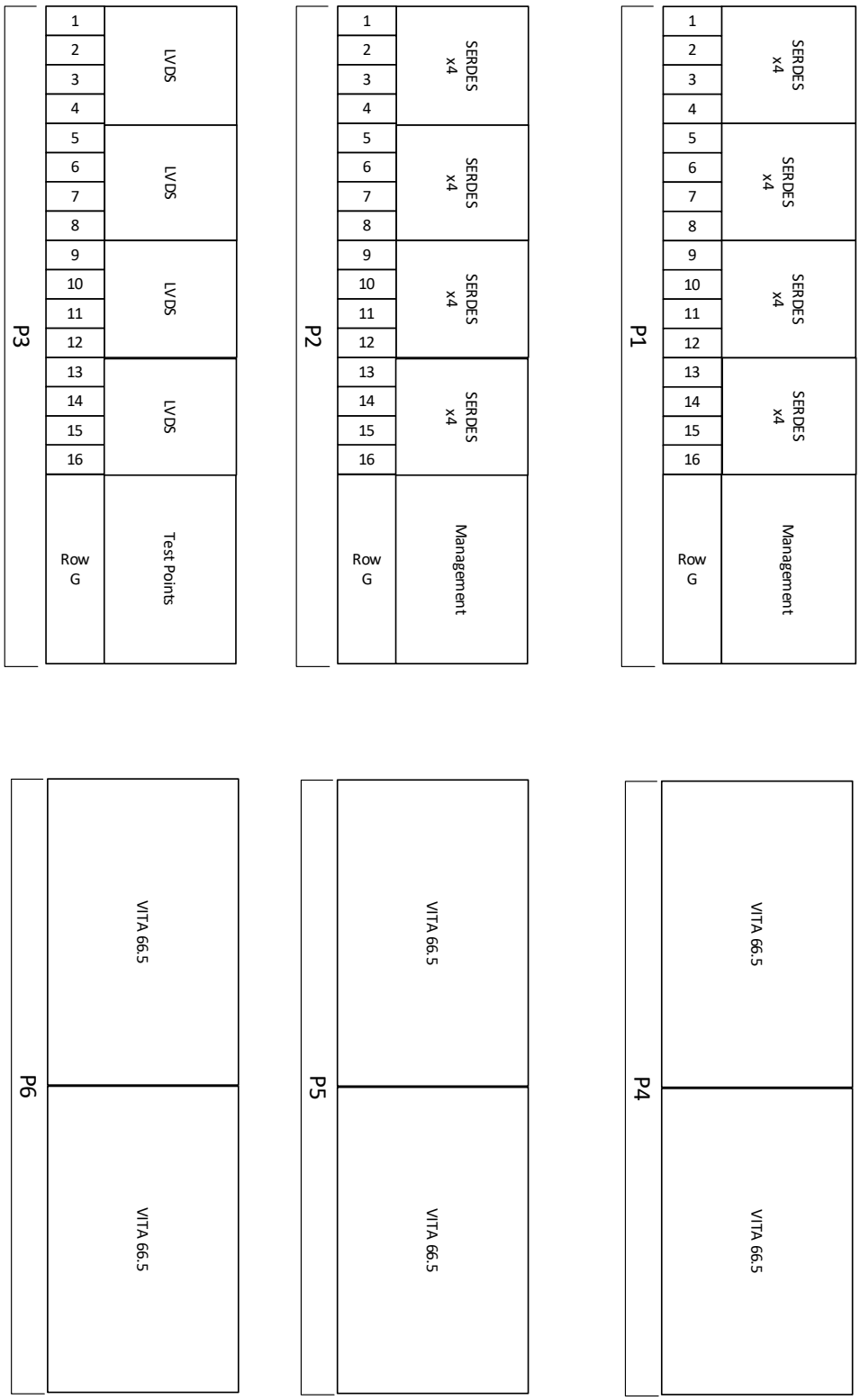


*Figure 4: VPX551 Backplane Pinout*

# Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

# Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

# Specifications

| | | |
|---|---|---|
| **Architecture** | | |
| **Physical** | **Dimensions** | 6U, 1” pitch |
| **Type** | **FPGA** | Dual Xilinx Kintex UltraScale™ XCKU115 |
| | **Memory** | 16 GB DDR4, 64-bit per FPGA |
| **Standards** | | |
| **VPX** | **Type** | VITA 46.x |
| **VPX** | **Type** | VITA 65 |
| **Module Management** | | OpenVPX Health Management |
| **Configuration** | | |
| **Power** | **VPX551** | ~120W |
| **Front Panel** | **JTAG** | Standard JTAG header |
| | **USB** | USB to FPGA |
| | **1/10GbE** | SFP+ |
| | **LEDs** | User defined from FPGA |
| | | Health Management Status |
| | **Switch** | Reset, push-button |
| **VPX Interfaces** | **Slot Profiles** | See Ordering Options |
| | **Rear IO** | P0: IPMB for Health Management |
| | | P1 and P2: Four SERDES x4 from each FPGA |
| | | P3: Sixteen LVDS from each FPGA |
| | | P4 to P6: Six VITA 66.5 |
| | **Power Supplies** | On P0: VS1/VS2 = 12V; VS3 = +5V |
| **Other** | | |
| **MTBF** | MIL Hand book 217-F@ TBD hrs | |
| **Certifications** | Designed to meet FCC, CE and UL certifications, where applicable | |
| **Standards** | VadaTech is certified to both the ISO9001:2015 and AS9100D standards | |
| **Warranty** | Two (2) years, see VadaTech Terms and Conditions | |

### INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

# Ordering Options

## VPX551 – ABC-DEF-GHJ-K00

| A = P4 VITA 66.5 | D = FPGA Speed | G = Applicable Slot Profiles | K = VPX Connector Type |
|---|---|---|---|
| See Table 1 | 1 = Reserved<br>2 = High<br>3 = Highest | 0 = 5HP, VITA 48.1<br>1 = Reserved | 0 = Standard 50u Gold Rugged<br>1 = KVPX Connectors |
| **B = P5 VITA 66.5** | **E = SFP+** | **H = Environmental** | |
| See Table 1 | 0 = No SFP+ txcvr<br>1 = 10GbE SR<br>2 = 10GbE LR<br>3 = DWDM<br>4 = 10GbE ER<br>5 = 100/1000/10000GbE (Copper) | See Environmental Specification | |
| **C = P6 VITA 66.5** | **F = PCIe on P1/P2** | **J = Conformal Coating** | |
| See Table 1 | See Table 2 | 0 = No coating<br>1 = Humiseal 1A33 Polyurethane<br>2 = Humiseal 1B31 Acrylic | |

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

| Option | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|---|
| Pn-UPR | None | None | None | TX | TX | TX | RX | RX | RX |
| Pn-LWR | None | TX | RX | None | TX | RX | None | TX | RX |

*Table 1: VITA 66.5 Transceiver Selection, two available per Pn position*

| Option | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|---|
| P1 | None | 0-3 | 0-7 | 0-11 | 0-15 | 0-15 | 0-15 | 0-15 | 0-15 | 0-7 |
| P2 | None | None | None | None | None | 0-3 | 0-7 | 0-11 | 0-15 | 0-7 |

*Table 2: PCIe Ports (Ports not terminated for PCIe can be used for protocols such as SRIO, XAUI or Aurora)*

Notes: Please contact VadaTech for more options.

## Environmental Specification

| | Air Cooled | | Conduction Cooled | | |
|---|---|---|---|---|---|
| **Option H** | **H = 0** | **H = 1** | **H = 2** | **H = 3** | **H = 4** |
| **Operating Temperature** | AC1* (0°C to +55°C) | AC3* (-40°C to +70°C) | CC1* (0°C to +55°C) | CC3* (-40°C to +70°C) | CC4* (-40°C to +85°C) |
| **Storage Temperature** | C1* (-40°C to +85°C) | C3* (-50°C to +100°C) | C1* (-40°C to +85°C) | C3* (-50°C to +100°C) | C3* (-50°C to +100°C) |
| **Operating Vibration** | V2* (0.04 g2/Hz max) | V2* (0.04 g2/Hz max) | V3* (0.1 g2/Hz max) | V3* (0.1 g2/Hz max) | V3 (0.1 g2/Hz max) |
| **Storage Vibration** | OS1* (20g) | OS1* (20g) | OS2* (40g) | OS2* (40g) | OS2* (40g) |
| **Humidity** | 95% non-condensing | 95% non-condensing | 95% non-condensing | 95% non-condensing | 95% non-condensing |

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4)

# Contact

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