

VPX571

Dual RF Agile Transceiver with
VITA 67.2 RF Connector, 3U VPX



VPX571

Key Features

- Dual RF transceiver (AD9364)
- Xilinx UltraScale+ XCZU15EG FPGA
- 8 GB of 64-bit wide DDR4 Memory (single bank) with ECC
- MPSoC with block RAM and UltraRAM
- RF routed as option to VITA 67.2
- Health Management through dedicated Processor

Benefits

- Integrated transceiver covering 70 MHz to 6 GHz
- 12-bit ADC/DAC
- Reference design with VHDL source code speeds application development
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™



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VPX571

The VPX571 provides dual integrated RF transceivers, each based on AD9364. One channel includes a programmable filter on transmit. The module is compatible with Analog Devices RadioVerse design tools.

The Module routes its RF as an option to the VITA 67.2 connector or to the front panel. The module has 8 TX/RX SERDES, Dual GbE, 8 LVDS (could be configured as singled ended), CPU RS-232 and management RS-232 to the P1 connector.

The FPGA has interface to a single DDR4 memory channel (64-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

VPX571 is based on Xilinx UltraScale+ XCZU15EG MPSoC FPGA, which has 3528 DSP Slices and 746k logic cells. The XCZU15EG includes quad-core ARM application processor, dual-core ARM real-time processor and Mali™ graphics processing unit, as well as over 26 Mb of block RAM and 31 Mb of UltraRAM.

The module has onboard 64 GB of Flash, 128 MB of Boot Flash and an SD Card as an option.



Figure 1: VPX571



Figure 2: VPX571 (without Front Panel)

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

[Xilinx Vivado Design Suite](#), [Xilinx System Generator for DSP](#).

Block Diagram

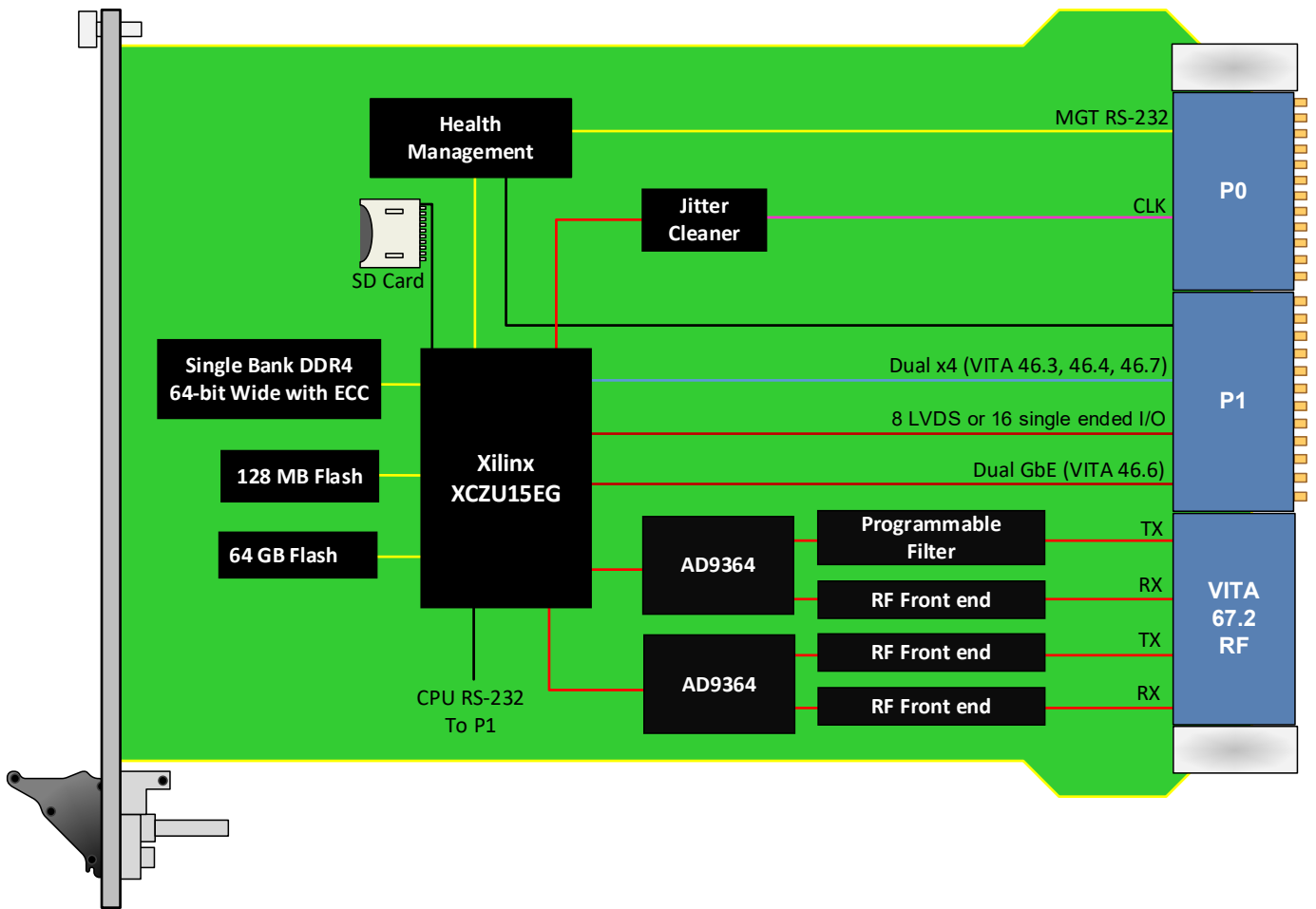


Figure 3: VPX571 Functional Block Diagram

Backplane Pinout

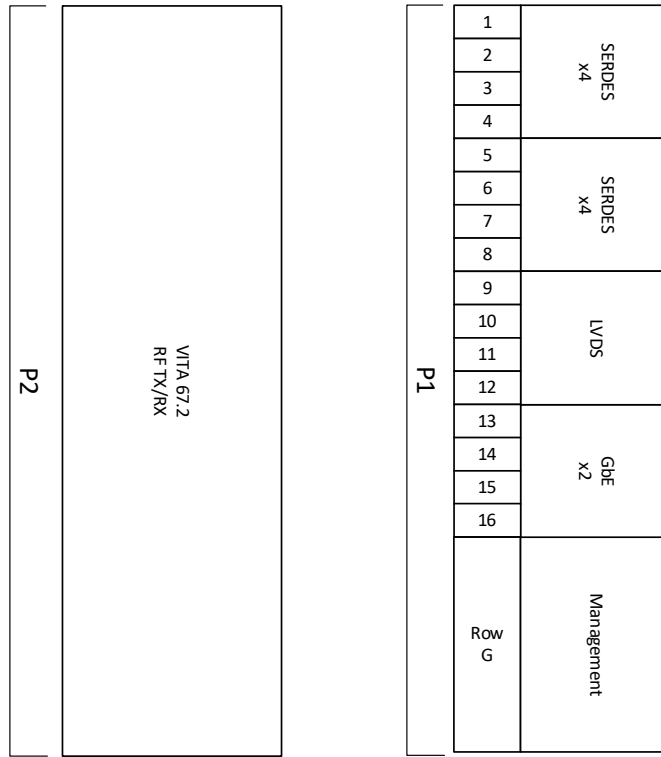


Figure 4: VPX571 Backplane Pinout

Specifications

| Architecture | | |
|--------------------------|-----------------------------|---|
| Physical | Dimensions | 3U, 1" pitch |
| Type | Controller | OpenVPX payload module with Health Management |
| Standards | | |
| VPX | Type | VITA 46.x, VITA 67.2 |
| VPX | Type | VITA 65 OpenVPX |
| Module Management | IPMI | IPMI v2.0 |
| Configuration | | |
| Power | VPX571 | ~50W (FPGA load dependent) |
| Front Panel | Interface Connectors | 8 LVDS or 16 singled ended I/O to P1 RTM management to P1 8 SERDES and dual GbE to P1 RS-232 from FPGA and RS-232 from Health Management to P1 |
| | LEDs | User defined by the FPGA and Health Management |
| VPX Interfaces | Slot Profiles | See Ordering Options |
| | Rear IO | Health Management, Clock and JTAG on P0 GbE, Serdes on P1 LVDS on P1 |
| Software Support | Operating System | Linux |
| Other | | |
| MTBF | | MIL Hand book 217-F@ TBD hrs |
| Certifications | | Designed to meet FCC, CE and UL certifications, where applicable |
| Standards | | VadaTech is certified to both the ISO9001:2015 and AS9100D standards |
| Warranty | | Two (2) years, see VadaTech Terms and Conditions |

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX571 – ABC-DEF-GHJ

| | | |
|--|--|---|
| A = RF Connector 0 = VITA 67.2 1 = Front panel | D = FPGA Speed 0 = Reserved 1 = High 2 = Highest | G = Slot Profile 0 = 5 HP, VITA 48.1 |
| B = SD Card 0 = No SD Card 1 = 32 GB | E = VPX Connector Type 0 = Standard 50u Gold Rugged 1 = KVPX Connectors | H = Environmental See Environmental Specification |
| C = Backplane LVDS 0 = LVDS routed to P1 1 = Not routed | F = PCIe Option (P1) for Data Port 1/2 0 = None/None* 1 = PCIe/None* 2 = None*/PCIe 3 = PCIe/PCIe | J = Conformal Coating 0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic |

Notes: *SERDES lanes that are not PCIe can be used for SRIO, XAUI or Aurora, depending on FPGA image.

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

| Option H | Air Cooled | | | Conduction Cooled | |
|------------------------------|----------------------|-----------------------|----------------------|-----------------------|-----------------------|
| | H = 0 | H = 1 | H = 2 | H = 3 | H = 4 |
| Operating Temperature | AC1* (0°C to +55°C) | AC3* (-40°C to +70°C) | CC1* (0°C to +55°C) | CC3* (-40°C to +70°C) | CC4* (-40°C to +85°C) |
| Storage Temperature | C1* (-40°C to +85°C) | C3* (-50°C to +100°C) | C1* (-40°C to +85°C) | C3* (-50°C to +100°C) | C3* (-50°C to +100°C) |
| Operating Vibration | V2* (0.04 g2/Hz max) | V2* (0.04 g2/Hz max) | V3* (0.1 g2/Hz max) | V3* (0.1 g2/Hz max) | V3 (0.1 g2/Hz max) |
| Storage Vibration | OS1* (20g) | OS1* (20g) | OS2* (40g) | OS2* (40g) | OS2* (40g) |
| Humidity | 95% non-condensing | 95% non-condensing | 95% non-condensing | 95% non-condensing | 95% non-condensing |

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX004



- Unified 1 GHz quad-core CPU for, Shelf Manager, and Fabric management
- Automatic fail-over with redundant VPX004
- 1GbE base switch with dual 100/1000/10G uplink

VPX752



- 6U VPX module Intel 5th Generation Xeon-D SoC
- PCIe Gen3 x 16 (dual x8 or Quad x4)
- Quad 10GbE XAUI

VTX870



- Open VPX benchtop development platform
- Dedicated Switch/management slot
- Up to five 3U VPX payload slots

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