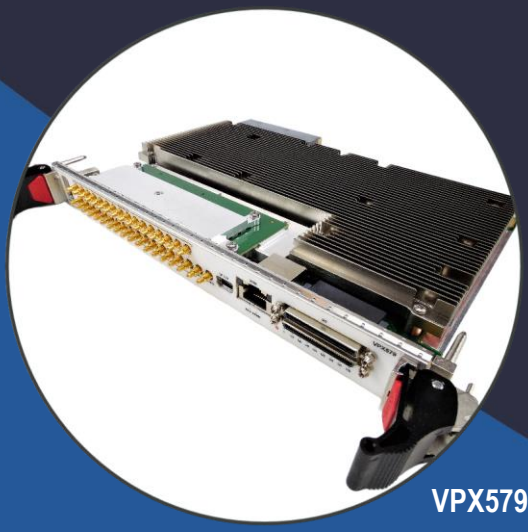
VPX579

3rd Generation Zynq RFSoC UltraScale+, 6U VPX



VPX579

Key Features

- 3rd Generation Xilinx RFSoC XCZU49DR
- 16 ADC and 16 DAC simultaneous processing
- Suitable for 5G/4G/LTE and SDR deployment
- 8GBytes of DDR-4 with ECC to PS
- 8GBytes of DDR-4 to PL
- MPSoC with block RAM and UltraRAM
- 64G SATA NANDrive
- 32 GPIO, 20 LVDS and 4x RS-485
- Health Management through dedicated Processor

Benefits

- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX579

The VPX579 is a 6U VPX RFSoC FPGA based on Xilinx XCZU49DR MPSoC FPGA with front I/O access. The module has an on-board, reconfigurable FPGA which interfaces directly to the VPX P1-P2 with high speed SERDES. The SERDES are configurable to run multiple protocols such as PCIe, Aurora, SRIO, XAUI, 40G, 100G, etc. For the PCIe option the module could run as single x16/x8/x4, dual x4/x4 or dual x8/x8.

The CPU (Processing System "PS") has interface to a single bank of DDR4 memory channel (64-bit wide with ECC) with total capacity of 8 GB. The PL (Programmable Logic) interfaces to 8GB of DDR-4. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host. The module has onboard 64 GB of SATA NANDrive Flash, 128 MB of Boot Flash, and an SD Card option.

The VPX579 has 16 ADC channels capable of sampling at 2.5GSPS and 16 DAC channels capable of sampling at 9.85 GSPS (the FPGA speed of -I2 ordering option can go up to 10GSPS).

The VPX579 provides Display Port (DP), 32 General Purpose I/O, 20 LVDS, and four RS-485 through the front panel. The I/O is provided via a High-Density Connector (HDC). There are three RS-232 ports that are routed to a RS-232 to a USB device. The module also has a GbE to the front panel from the PS.

Onboard microcontroller implements Tier-2 health management.

Figure 1: VPX579

Block Diagram

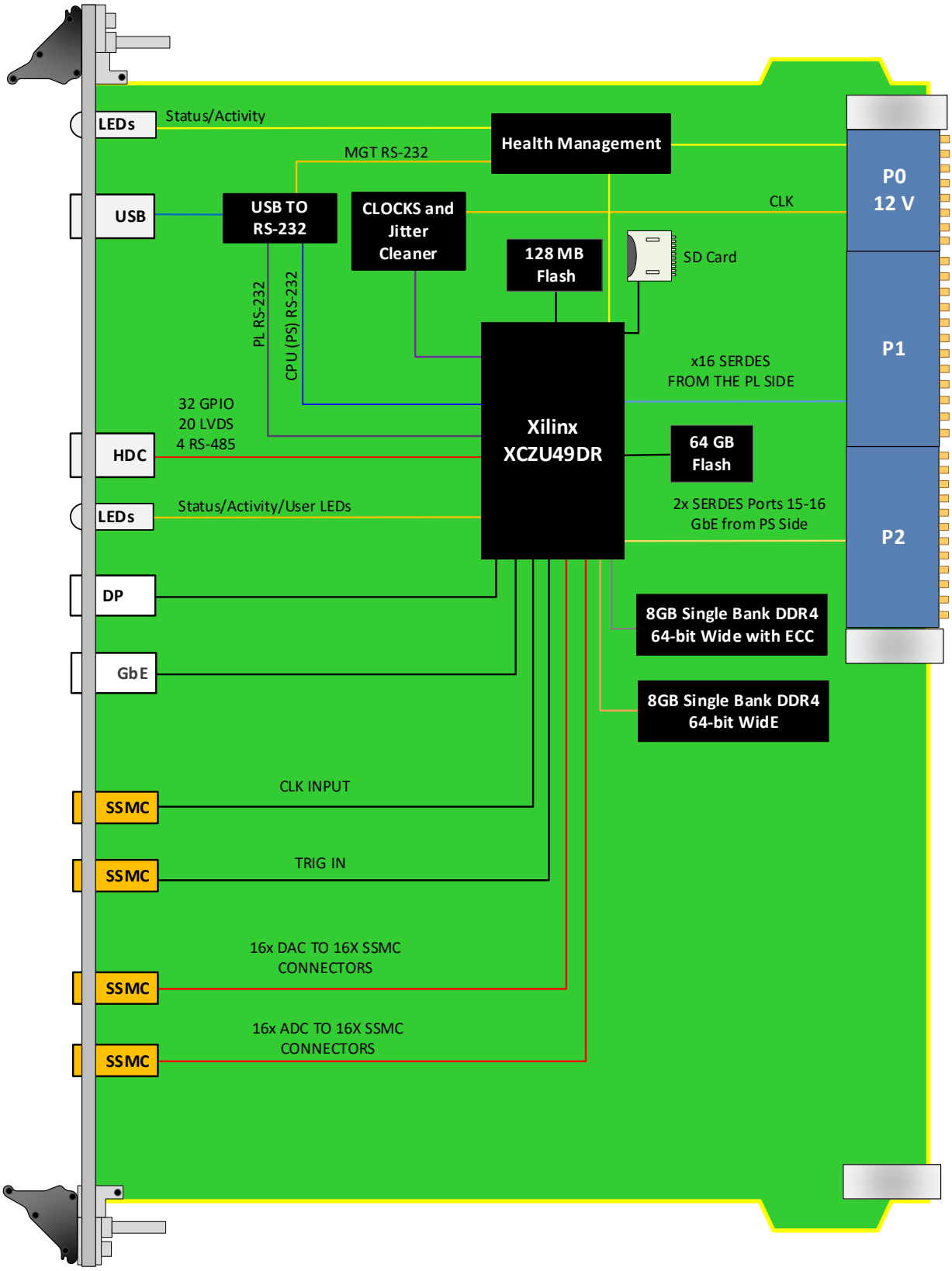
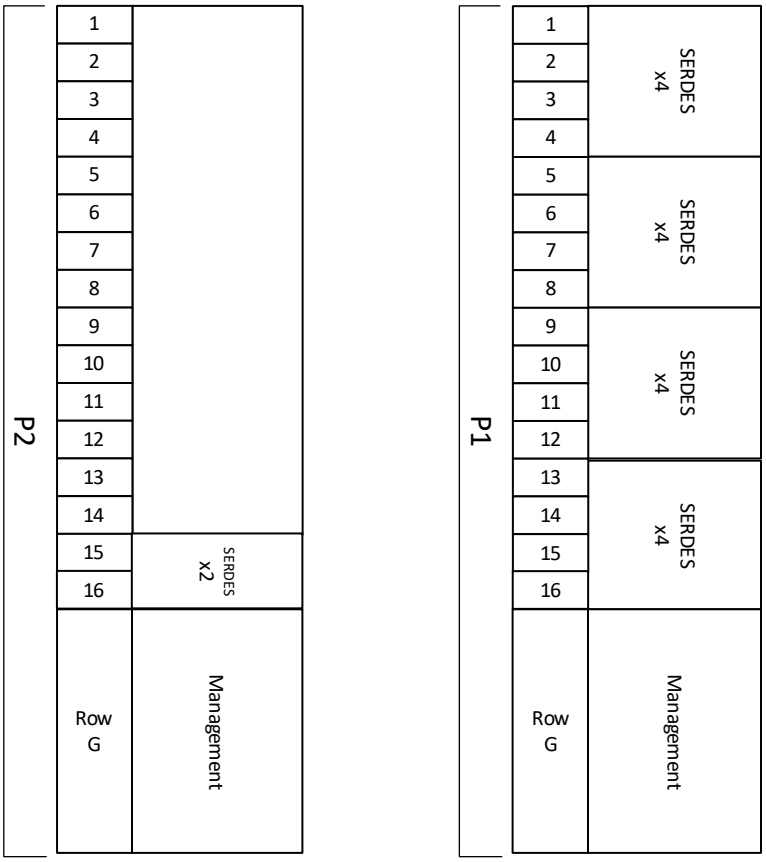


Figure 2: VPX579 Functional Block Diagram

Pinout Block Diagram



Front Panel

Figure 3: VPX579 Front Panel View

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	6U, 1” pitch
Type	**FPGA**	Xilinx Zynq RFSoC UltraScale+
Configuration		
Power	**VPX579**	50W FPGA load dependent
Front Panel	**Interface Connectors**	GbE via RJ-45
		3x RS-232 to USB
		32x GPIO, 20x LVDS, and 4x RS-485 via high density connector
		Display Port via Mini DP
	LEDs	User defined by the FPGA and Health Management
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	P0: IPMB for Health Management and CLK
		P1: 16x High speed SERDES
		P2: 2x GbE to the PS
Software Support	**Operating System**	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX579 – ABC-DEF-GHJ-K

A = VPX Connector Type	D = FPGA Speed	G = Applicable Slot Profiles	K = Front End Balun
0 = Multigig RT3 50u Gold Rugged 1 = KVPX Connectors	1 = Reserved 2 = High (-2) 3 = Reserved 4 = High (-2I)**	0 = 5 HP, VITA 48.1	0 = 10 to 4000MHz** 1 = 10 to 3000MHz 2 = 500KHz to 6000Mhz**
B = Expansion Plane (P2)*	**E = 32 GPIO Voltage rating**	**H = Environmental**	
0 = P2 Not loaded 1 = P2 Loaded	0 = +3.3V for all 32 I/O 1 = +5V for all 32 I/O 2 = +3.3V for 16 I/O and +5V for 16 I/O	See Environmental Specification	
C = SD Card	**F = PCIe Option (P1)**	**J = Conformal Coating**	
0 = No SD Card 1 = SD Card (32 GB) 2 = SD Card (64 GB)	0 = No PCIe 1 = PCIe 1-4 ports (PCIe x4) 2 = PCIe 1-8 ports (PCIe x8) 3 = PCIe 1-16 ports (PCIe x16)	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic	

* For RTMs that utilize the P2 connector signals, ordering option B=1 must be selected

**-2I speed grade can do 10GSPS for the DAC side, minimum order qty is needed

** Minimum order qty needed

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX592

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

Contact

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