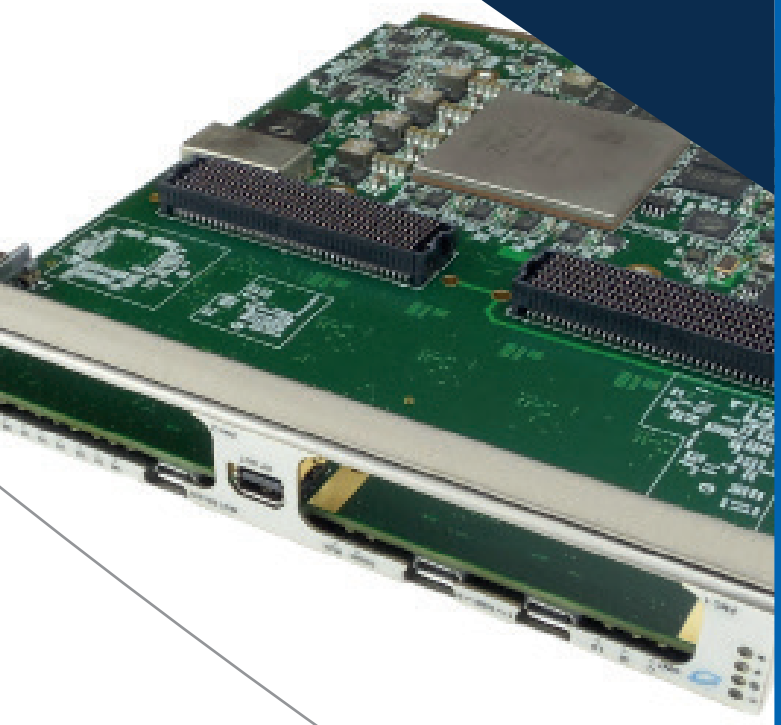
Solution Brief

Real-Time Motion Control Platform

AMC580 Zynq UltraScale+ EG



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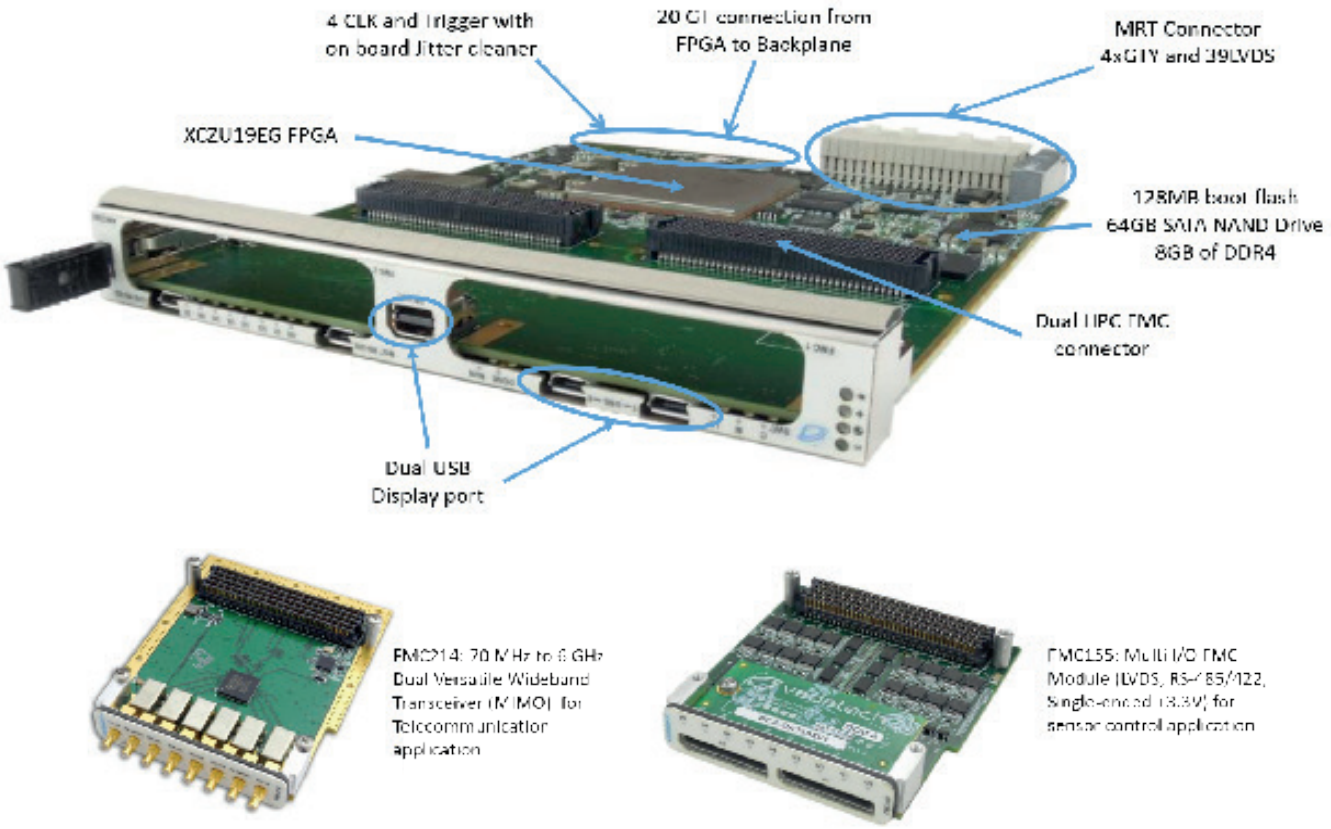
Executive Summary

Based on the Xilinx Zynq ® UltraScale+ XCZU19EG FPGA, VadaTech's AMC580 provides the most complete and powerful MPSoC (Multi Processor System on Chip) on the market. With its quad-core ARM ® Cortex-A53 for processing, dual-core Cortex-R5 for real time application, linked via a very high-speed interconnect to a 1.143 million logic cells FPGA, the AMC580 brings scalable open form-factor architecture to the level required by most demanding application:

- motion-control
- latest telecommunication standards and measurement
- medical devices
- particle accelerators

The AMC580 offers the best performances in terms of connectivity with 20 GTH, 154 LVDS pairs to the front dual HPC FMC connectors, 4 GTY, 39 LVDS pairs to the MRT connector, and 18 GTH to the backplane. Based on Vita-47 and MTCA.4 open standards, it is possible to design or use existing standard daughter card for sensor and control application interface.

AMC580 and the Zynq UltraScale+ 19EG overview

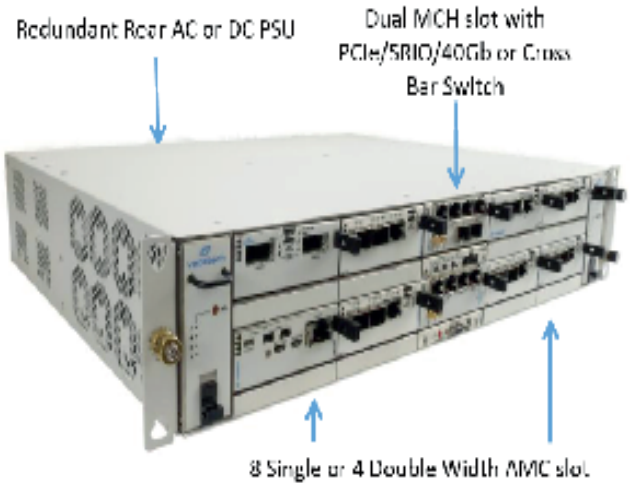


Item	Key Features	Application
• Programmable Logic	• PCIe, SRIO, XAUI, 40GbE, AURORA compatible • System Logic Cells (K): 1,143 • Memory (Mb): 70.6 • DSP Slices: 1,968	• Very High interconnect and signal processing
• Quad-core ARM Cortex-A53	• 64-bit architecture running up to 1.5GHz • 2.3 DMIPS/MHz performance • 8GB DDR4 memory with ECC	• Processing Unit for high-performance control
• Dual-core ARM Cortex-R5	• ARMv7 32-bit architecture running at up to 600MHz • 1.67 DMIPS/MHz performance • Lock-step mode for high reliability	• Safety critical systems (SIL3 safety), real-time I/O and algorithms
• ARM MaliTM-400 MP2	• Multicore 2D/3D acceleration at 667MHz • 1080p resolution graphics • OpenGL ES 1.1 and 2.0 • OpenVG 1.0 and 1.1	• Ideal for multimedia, Automotive ADAS, and surveillance applications.

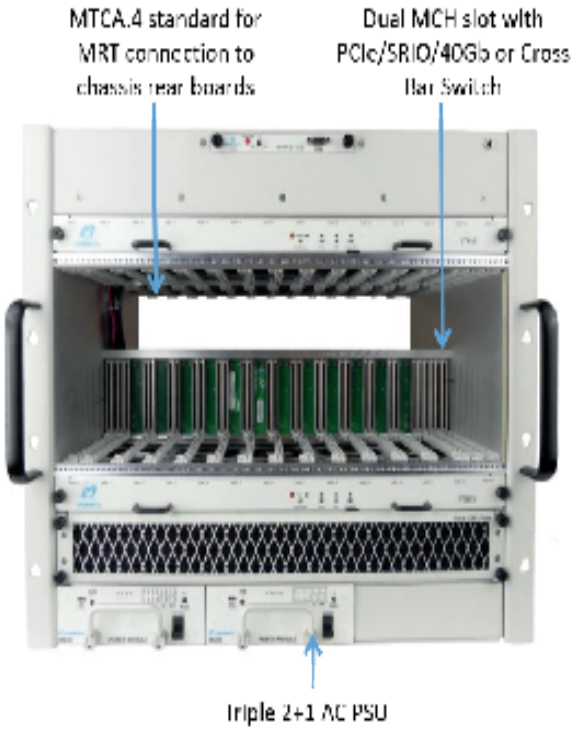
Adding the crates with protocol configurable switch

Combining all the advantages of MicroTCA form-factor for Size, Weight, Power and Cost (SWAP-C) with the latest technology from Xilinx, VadaTech provides a scalable and fully redundant platform for the highest demanding applications. Our chassis portfolio includes solution from 1U to 9U, with below examples based on the 2U chassis VT812 and 9U VT815.

2U, 19" crates
VT880/VT881/VT812



9U, 9", 12 slots crate VT815



A Management Carrier Hub (MCH) includes the switches connecting up to twelve (12) boards together within one crate via the backplane. It also provides I/O and networking interfaces on its front panel. The MCH can be ordered with different switch options to match the protocol used to communicate between the boards in thte crate.

Most MCH products from commercial vendors are limited to standard bus protocols such as PCI Express, Serial RapidIO, and 10/40 Gigabit Ethernet (GbE). Even though these protocols have exceptional throughput capability, they are neither deterministic nor necessarily low-latency. VadaTech delivers its UTC004 MCH with a user-configurable switch fabric that overcomes this limitation, offering the system architect/developer complete flexibility in both interface protocol and the routing of information between blades on top of embedded Timing functionalities.

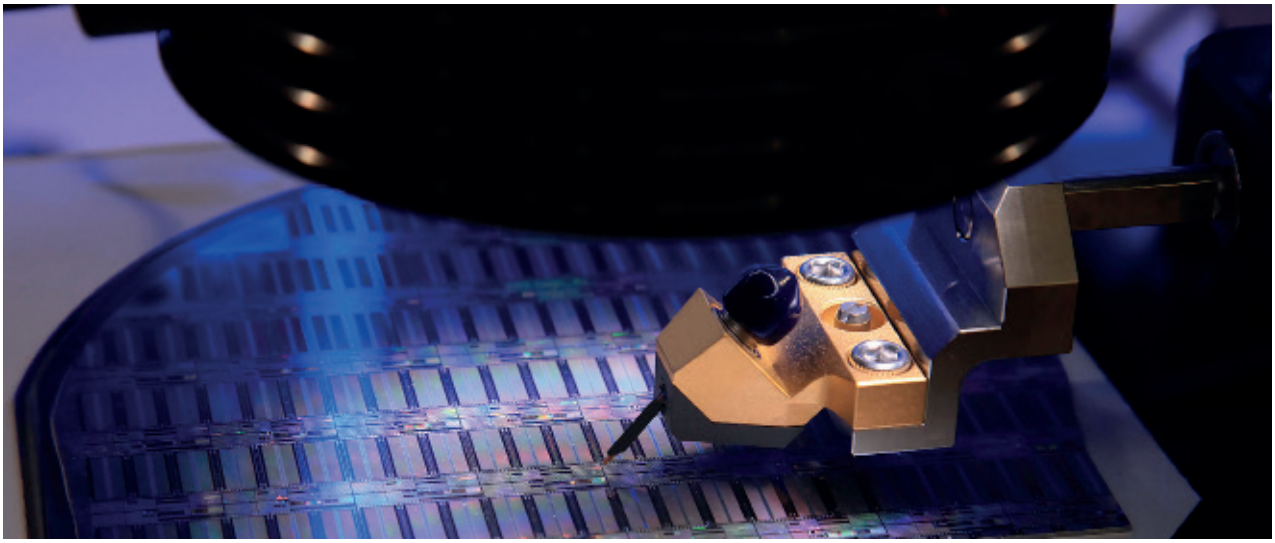
AMC580 on vadatech.com

MCH UTC004 on vadatech.com

Application Case

Typical automation/motion control applications require multi-board systems with each board doing one function (IO, Control CPU, Communication CPU, FPGA processing, motor control). The complexity of these architectures makes it hard to reach the system reliability target as well as the low/deterministic latency between each node.

To meet with the higher standards of security and reliability of the Automation industry, VadaTech designed a 2U platform based on the VT812 that provides full redundancy in Power Supply, Fan and Switch. In addition of a diminution of the power consumption of the system, our architecture based on MPSoC enables a bandwidth that is not reachable with multichip solutions.



Advantages of AMC580 for next generation of motion sensor systems

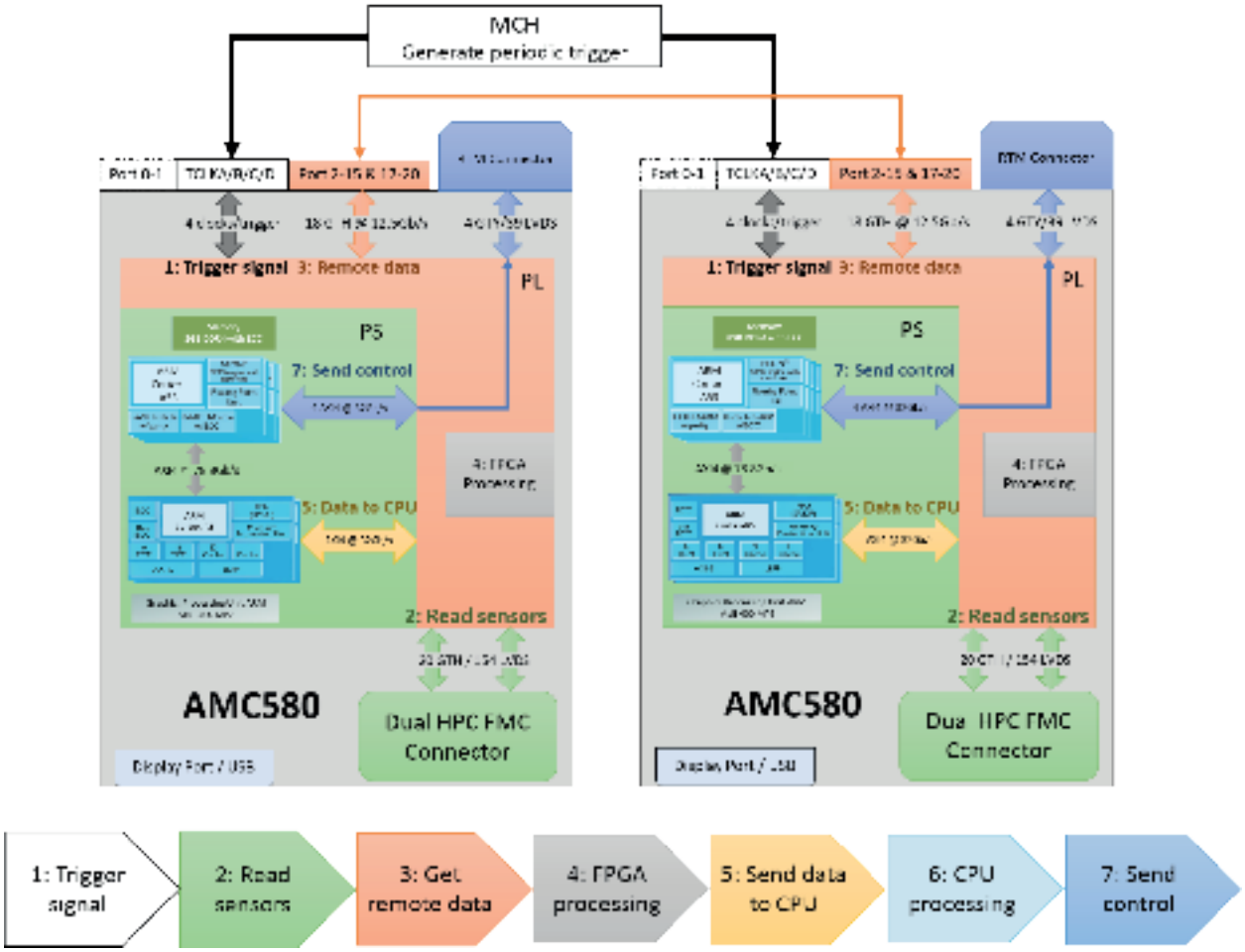
In order to analyze the performance an architecture based on AMC580 we evaluate the following simplified motor control process:

- A periodic signal (ex. every 1ms) and a reference clock are generated by the MCH and distributed to all the AMC580 via TCLKA.
- At the trigger signal, all AMC580 initiate a sensors read.
- Data are exchanged between the AMC580 to synchronize their status.
- A FPGA processing is done based on sensors data and remote data (ex. filter, correlation, etc.).
- The FPGA sends data to the ARM Cortex-R5 and ARM Cortex-A53 CPU (ex. result of processing)
- The CPU launches the control algorithm based on data received from the FPGA.
- The CPU updates the motor control via the RTM

In order to have a reliable control system, the complete chain has to finish before the next trigger signal (ex. 1ms budget). In our case, we analyze a Hard real-time control system (missing a deadline is considered a total system failure). Which mean that for each step of the control process, we need to determine the worst case.

We compare our architecture with a typical architecture based on one board for each function:

- I/O boards (sensors)
- FPGA boards (processing)
- 1CPU boards (processing)
- I/O boards (motor-control)
- SRIO switch



The AMC580 based system can have a total communication latency below 500ns. Which in this application case give a budget of 999.5us for the CPU and FPGA processing.

The multi-board system has a total communication latency around 1us. A more powerful CPU can compensate the smaller processing budget. But the system designer's task to prove Hard real-time will be harder as the system is less deterministic as detailed in the table next page.

Advantages of AMC580 for next generation of motion sensor systems

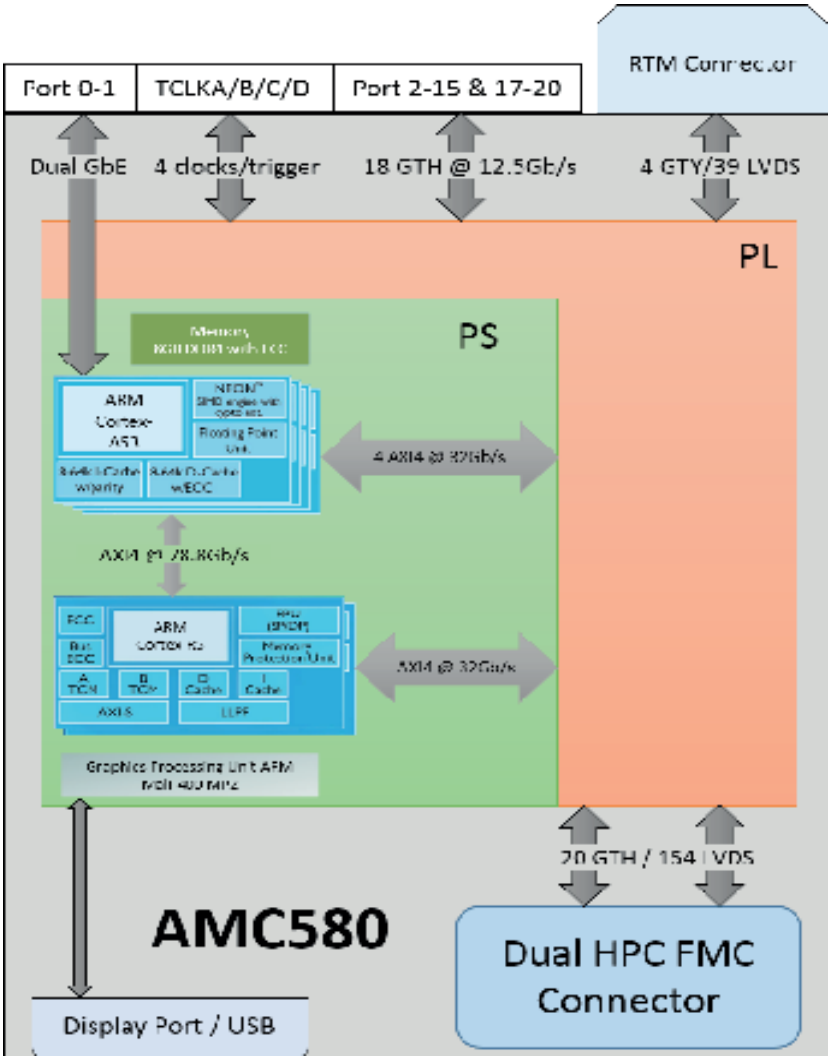
Step	AMC580	Typical architecture	Advantage of AMC580 for next gen
1. Trigger signal	The synchronous trigger signal is received by the FPGA and sampled on the reference clock.	The synchronous trigger signal is received by the FPGA and sampled on the reference clock.	Both systems are equivalent
2. Read sensors ++	The FPGA reads sensors values via the FMC connectors (direct LVDS connection). Latency can be as low as 10ns for a 100MHz refresh rate sensor.	The FPGA reads the current sensor value via SRIO. The total latency includes the SRIO path and the sensor latency. Latency can be as low as 250ns.	Direct sensors sampling allows 10x lower latency. The jitter is also minimum (no SRIO switch between the FPGA and the sensor).
3. Get remote data ++	Each FPGA has a direct connection to all the other FPGA. The protocol can be SRIO, Aurora or other. Each direct link is up to 12.5Gbps.	Each FPGA has a 4x connection to a SRIO gen2 switch.	Both systems are equivalent in term of number of lanes, as they both use the maximum number of Fabric lanes of the backplane. For example, a system with four FPGA with a dedicated 4x connection to a central switch is equivalent to a system with four FPGA with 1x direct connection between them (in the case where all the FPGA send a message to all the other FPGA). However, the SRIO gen2 is limited to 6.25Gbps while the direct connection is rated up to 12.5Gsps.
4. FPGA processing	The Xilinx Zynq Ultrascale+ 1968 DSP slices can run at up to 600MHz.	Idem (for Xilinx 7 Series FPGA solutions).	Both systems are equivalent.
5. Send data to CPU ++	The FPGA sends data to the CPU via an AXI4 bus (128bit wide, at 250MHz). The ARM Cortex-R5 has fast interrupt line controlled by the FPGA. The latency can be as low as 10ns for a 128bit payload.	The FPGA sends data to the CPU via a SRIO 4x connection. Latency can be as low as 250ns.	The direct connection between the FPGA and the CPU allows a huge gain in latency and latency jitter. The ARM Cortex-R5, with its TCM memory allows low latency interrupt.
6. CPU processing	The ARM Cortex-R5 CPU is coupled with TCM memory, which allows the design of application with very low execution time jitter (TCM memory access time are deterministic). For intensive algorithm, the ARM Cortex-A53 can be used. The FPGA can directly write data to the TCM memory or the ARM Cortex-A53 L1 cache.	A high performance CPU can be used. The latest CPU from Intel or AMD can provide a huge throughput. But the designer needs to carefully analyze the worst case execution time, as execution time jitter can be high (a cache miss can add up to 100ns execution time), and interrupt latency/jitter is higher than the ARM Cortex-R5.	A separated CPU board gives the designer access to the most powerful CPU. However, these CPU will be harder to program, as the designer need to take into account the variability in execution time.
7. Send control ++	The CPU sends the control data to the RTP via an AXI4 (128bit wide at 250MHz). The latency can be as low as 10ns for a 128bit control word.	The CPU sends the control word to the I/O board via SRIO 4x. Latency can be as low as 250ns.	The direct connection between the control I/O and the ARM Cortex-R5 CPU allows a huge gain in latency.

AMC580 detailed architecture

The AMC580 versatile architecture incorporates all the nodes required for Automation in a Single Board design.

The two HPC FMC connectors associated with the RTM connector provide 193 LVDS pairs (or 386 CMOS lanes) to the sensors / motor control IO boards. 24 GT are also available for high throughput sensors/ networking (up to 300 Gbps full duplex data rate). These interfaces are directly connected to the FPGA logic, which allows the system architect to design complex/computation intensive pre-processing (filters, FFT, correlator, modulators, etc).

The FPGA section is also connected to the high speed backplane Fabric via the port 2-15 and 17-20. This allows board to board communication with up to 225Gbps full duplex data rate. A wide range of protocol is available (PCIe gen3, SRIO, Aurora, 40GbE, custom).



The Zynq Ultrascale+ MPSoC links the FPGA section to a complete compute unit, with a Quad-core ARM Cortex-A53, a Dual-core ARM Cortex-R5 and an ARM Mali-400MP2 Graphic Processing Unit.

The Dual-core ARM Cortex-R5, associated with 256KB of Tightly-coupled memory (deterministic/low-latency memory), as well as an optional lockstep mode makes this compute unit ideal to run safety-critical / real-time functions. A high speed AMBA AXI4 bus (up to 32Gbps full duplex) and low latency interrupts to the FPGA section allow deterministic transfer of data between the two compute units.

Cortex RTOS for AMC580

The Quad-core ARM Cortex-A53 running at up to 1500MHz provides the computational power required by high performance control application. This compute unit is associated with 8GB of DDR4 memory with ECC. A high speed AMBA AXI4 bus to the Dual-core ARM Cortex-R5 and the FPGA section, with its integrated DMA engine allows complex data movement between the compute units (up to 200Gbps full duplex cumulated data rate). Remote access to the Quad-core ARM Cortex-A53 is available via the dual GbE connection to the backplane.

The ARM Cortex-R5 and ARM Cortex-A53 are compatible with bare-metal application, as well as the majors RTOS:

Vendor	Product	Cortex-A53	Cortex-R5	Safety-Certifiable
Xilinx	Bare-Metal	Y	Y	Customer-dependent
Xilinx/RTEL	FreeRTOS	Y	Y	N
DDC-I	Deos	Y	-	Y
eForce	uC3	Y	-	Y
Enea	OSE	Y	-	Y
eSOL	eT-kernel	Y	-	Y
Green Hills	Integrity-178	Y	N	Y
Green Hills	Integrity	Y	N	Y
Mentor	Nucleus	Y	Y	Y
Solicon Labs	uc/OS-II	Y	Y	Y
Silicon Labs	uc/OS-II	Y	Y	N
QNX	Neutrino	Y	N	Y
Sciopta	Sciopta RTOS	Y	Y	Y
Sysgo	PikeOS	Y	N	Y
Wind River	VxWorks	Y	Y	Y

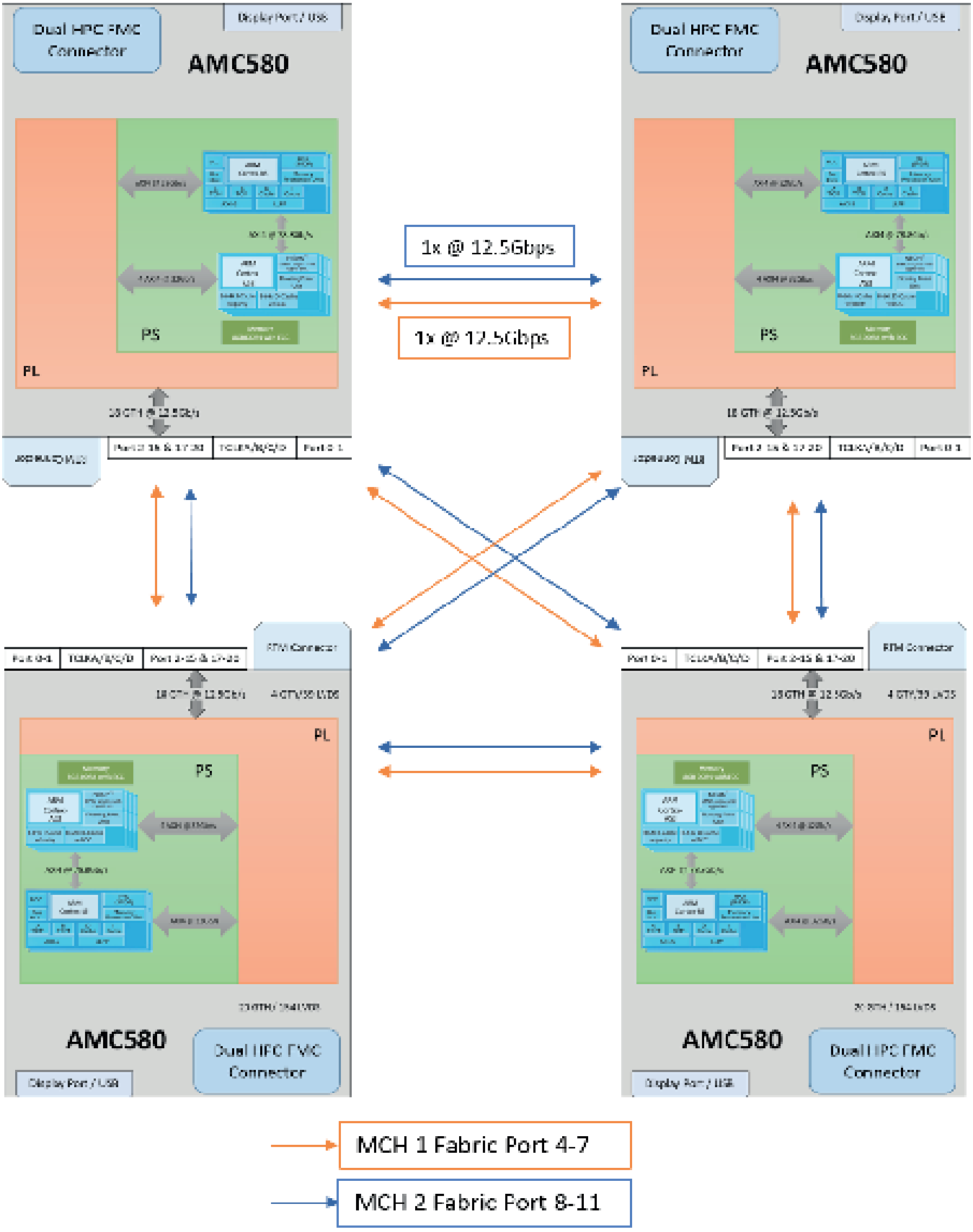
Data provided in above table for indication only. User shall verify with related vendors.

High-speed protocol inter-board connectivity in 2U 19" crate

Inter-blade communication is handled by two 12x12 full-duplex crossbar switches. Each communication port within the switch is comprised of four high-speed serial links.

These links are implemented on Ports 4-7 on MCH1 and Ports 8-11 on MCH2 of the MicroTCA switch fabric. By using the switch fabric, the Dual UTC004 (MCH) eliminates the need for rear-panel transition modules and front-panel fiber-optics to handle module-to-module communications. From a purely hardware perspective, the crossbar switchs are connected to the MicroTCA backplane as if they were a standard MCH module, capable of handling IPMI as well as any communication protocol (Aurora, PCie, SRIO, 40GbE). The UTC004 enable high speed deterministic direct link from board to board for IO sensor sharing, at a line rate up to 12.5Gbps.

High-speed protocol inter-board connectivity in 2U 19" crate



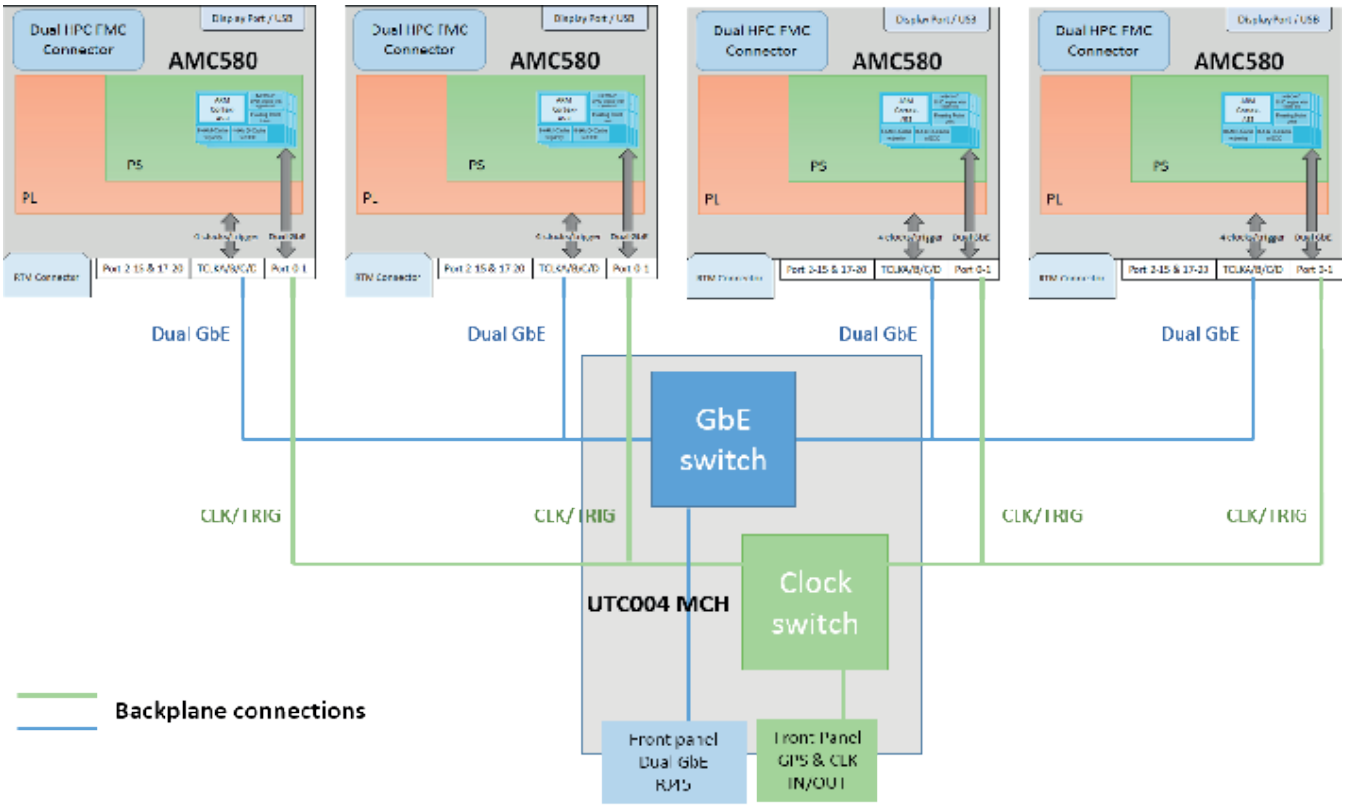
Lower critical control over GbE, Advanced timing distribution for synchronization

The UTC004 MCH includes a GbE switch connected to its front panel dual GbE RJ45. This GbE switch is also connected via the crate backplane to two ports on each slots of the crate. This allows the FPGA located in any slot to be fully monitored/programmed remotly.

The UTC004 MCH includes a clock switch connected to its front panel clock I/O with up to four clock and trigger signals dispatched to all the FPGA and other boards located in any slot of the crate. This standard architecture allows the system architect to create a redundant timing control unit.

The UTC004 MCH supports the following GPS and general-purpose clocking features:

- GPS receiver enables direct time/clock synchronization to the GPS satellite constellation
- Built-in GPS receiver for time/location/clock synchronization plus a DC-coupled LVCMOS Input / Output
- IEEE1588, PTP AND NTP Grand Master Clock
- Synchronous Ethernet JTAG Master / JTAG via Ethernet Virtual Probe



References of hardware part numbers

Contact your local Sales to request information about the new Automation platform including:

VadaTech P/N	Description	Available qty per SRIO platform	Available qty per CBS Platform	Available qty per CBS/SRIO Platform
VT812-200-011-000	2U uTCA.4 Chassis with 8 AMC Slots; Dual 500W AC (UTC017) Power Module; 1+1 Redundant (One primary and one redundant PM); Single module, mid-size (AMC5-6); Double module, mid-size (AMC7-8); JSM Installed; Commercial Temp Range; No Conformal Coating	1	1	1
UTC004-200-320-100-100	MCH for uTCA Chassis (3rd Generation); SRIO Gen 2 w/ QSFP+ Uplink; No SFP+ or QSFP+ Transceiver; Fabric not 10/40GbE; Built in GPS Receiver + LVCMOS in/Out; General-purpose M-LVDS clock matrix routed to backplane CLK3/FCLKA channels; Standard (XO) Clock holdover Stability; JTAG Virtual Probe included; MTCA.0 (Base specification, Air-cooled); Commercial Operating Temp, No conformal Coating; VadaTech stack (Switching protocols only)	2	0	1
UTC004-600-320-100-100	MCH for uTCA Chassis (3rd Generation); Cross Bar Switch (CBS) w/ QSFP+ Uplink; No SFP+ or QSFP+ Transceiver; Fabric not 10/40GbE; Built in GPS Receiver + LVCMOS in/Out; General-purpose M-LVDS clock matrix routed to backplane CLK3/FCLKA channels; Standard (XO) Clock holdover Stability; JTAG Virtual Probe included; MTCA.0 (Base specification, Air-cooled); Commercial Operating Temp, No conformal Coating; VadaTech stack (Switching protocols only)	0	2	1
AMC759-112-000-000	Intel Xeon E3 Processor AMC, SRIO; 16GB DDR4; 64 GB Flash; Mid-size; Commercial Operating Temp, No conformal Coating;	1	0	1
AMC580-002-120-000	Zynq UltraScale+ FPGA, Dual FMC Carrier, AMC; Not routed; Not routed; Mid-size; 32GB; High; No PCIe; Standard (XO); Commercial (–5° to +55° C), No coating	4	4	4
FMCs	Depending on customer application (Automation/Telecom/SIGINT)	Up to 8	Up to 8	Up to 8

Share your requirements with our Sales team and benefit from VadaTech's power of vision.

Check also:

[1] FMC214 datasheet for AD9361 ADC/DAC

[2] FMC230 datasheet for AD9371 and AD9375 ADC/DAC

[3] FMC155 datasheet for HPC I/O

[4] AMC585 datasheet for ZU19EG single width AMC

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