Solution Brief

Trigger synchronization and phase coherent in high speed multi-channels data acquisition system

Executive Summary

Trigger synchronization and phase coherent acquisition over multiple Data Acquisition Systems (DAQ) is critical to applications such as radar, electronic warfare and high energy physics. The latest GSPS ADCs, with sub-nanosecond acquisition period, make the trigger synchronization and phase alignment of multiple acquisition AMCs very challenging to achieve.

During the integration many factors can influence the synchronization of multi-channel acquisition system. These factors can be external to the digitizer platform such as the length of cables, or internal such as the backplane and PCB trace routing. It is thus necessary for the integrator to know the phase jitter they can expect from a platform and to be able to re-establish a synchronization after integration with external elements.

VadaTech Data Acquisition DAQ Series™ product line has been enhanced to answer this challenge, and make high density synchronized acquisition at very high speed a reality.

In the following document, we demonstrate the synchronization of two very high speed DAQ AMCs, with an accuracy of up to + - 0.5ps.

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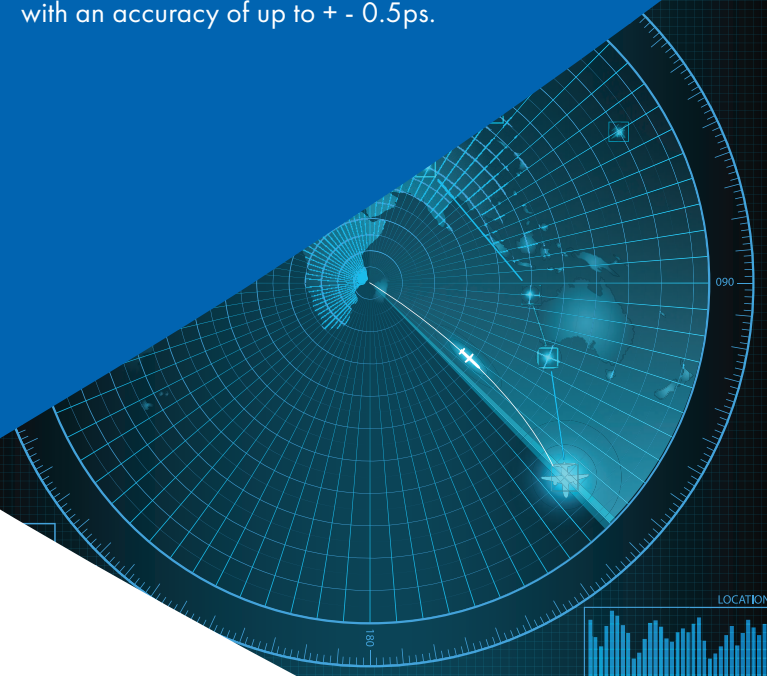
Method

The first step consist of setting the multiple clocks used in the acquisition boards with a deterministic phase relative to the reference clock of the system. This is achieved by a proper configuration of the PLL in each acquisition board.

In a second step the user optimizes the time window of arrival of the TRIGGER signal (triggering the acquisition over the multiple boards) and the JESD204B frame pulse (protocol used to transfer the digitized data between to the FPGA and DAQ) to provide a deterministic sampling of these signal across the multiple acquisition boards.

Finally the user adjusts the phase relation between the acquisition boards using accurate fine delays and VadaTech enhanced DAQ Series™ interface.

This method has to be typically performed only once during or after the integration.

Acquisition System Architecture

The demonstration acquisition system is composed of the following items:

- VT866 chassis (5U, PCIe gen3 capable, 12 slots chassis)
- UTC002 MCH
- AMC004 Reference clock / Trigger generator
- AMC516 – FMC225 (1 channel 4GSPS ADC)
- AMC517 – FMC226 (2 channels 4GSPS ADC)
- AMC726 running VadaTech DAQ Series™ Input Output Controller (IOC)
- Remote computer running VadaTech enhanced DAQ Series™ Graphical User Interface

Deterministic synchronized acquisition requires a common reference clock, as well as a fixed phase difference between the trigger signal and the reference clock. These requirements are met by using the AMC004 as a reference clock / trigger generator, with the clock routing capabilities of the VT866 chassis and the UTC002 MCH.

The AMC004's 10MHz reference clock is routed to the backplane TCLKA. The UTC002 clock Cross Bar Switch routes this reference clock to the AMC516 and AMC517 TCLKA.

The Acquisition input signal is distributed to the FMC225/FMC226 via a RF splitter, and length-matched cables (to give phase alignment of the two input signals).
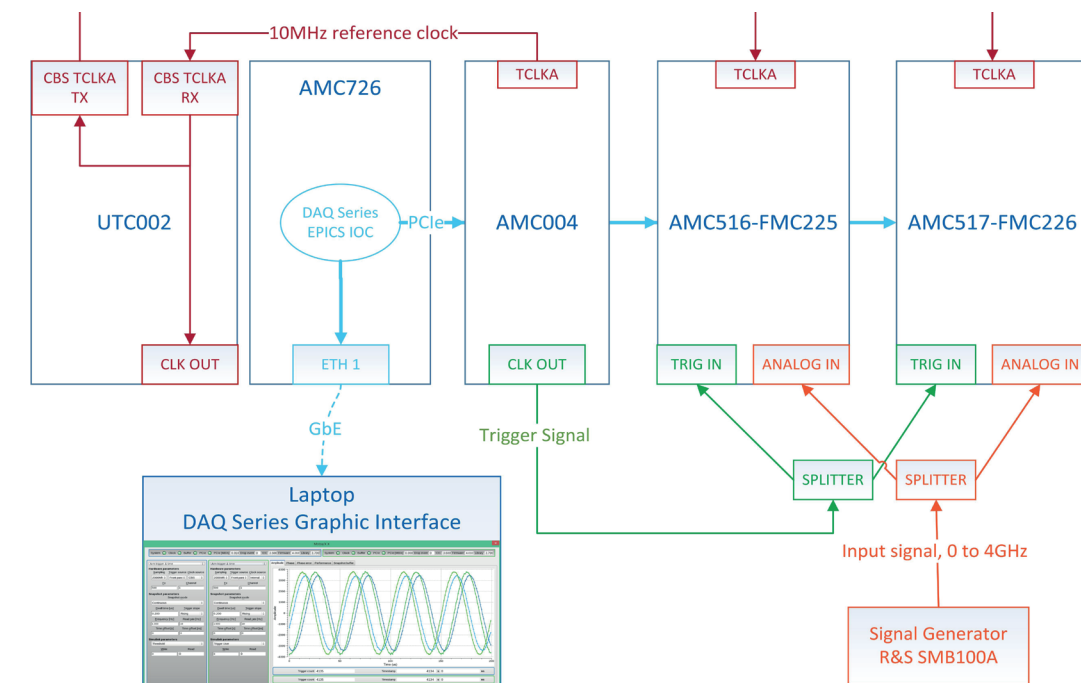

VT866
5U μTCA Chassis,
12 Full Size AMC, 40GbE

Figure 1: Synchronized DAQ Architecture

The AMC004's time trigger function generates a trigger event at a given GPS time. This trigger signal has a deterministic phase relationship to the 10MHz reference clock. The trigger generator is controlled over PCIe by the DAQ IOC running on the AMC726. The trigger signal is routed from the AMC004 front panel (CLK OUT) to the FMC225/FMC226 front panel (TRIG IN). The cable lengths between the trigger splitter and the FMC225/FMC226 TRIG IN are the same length.
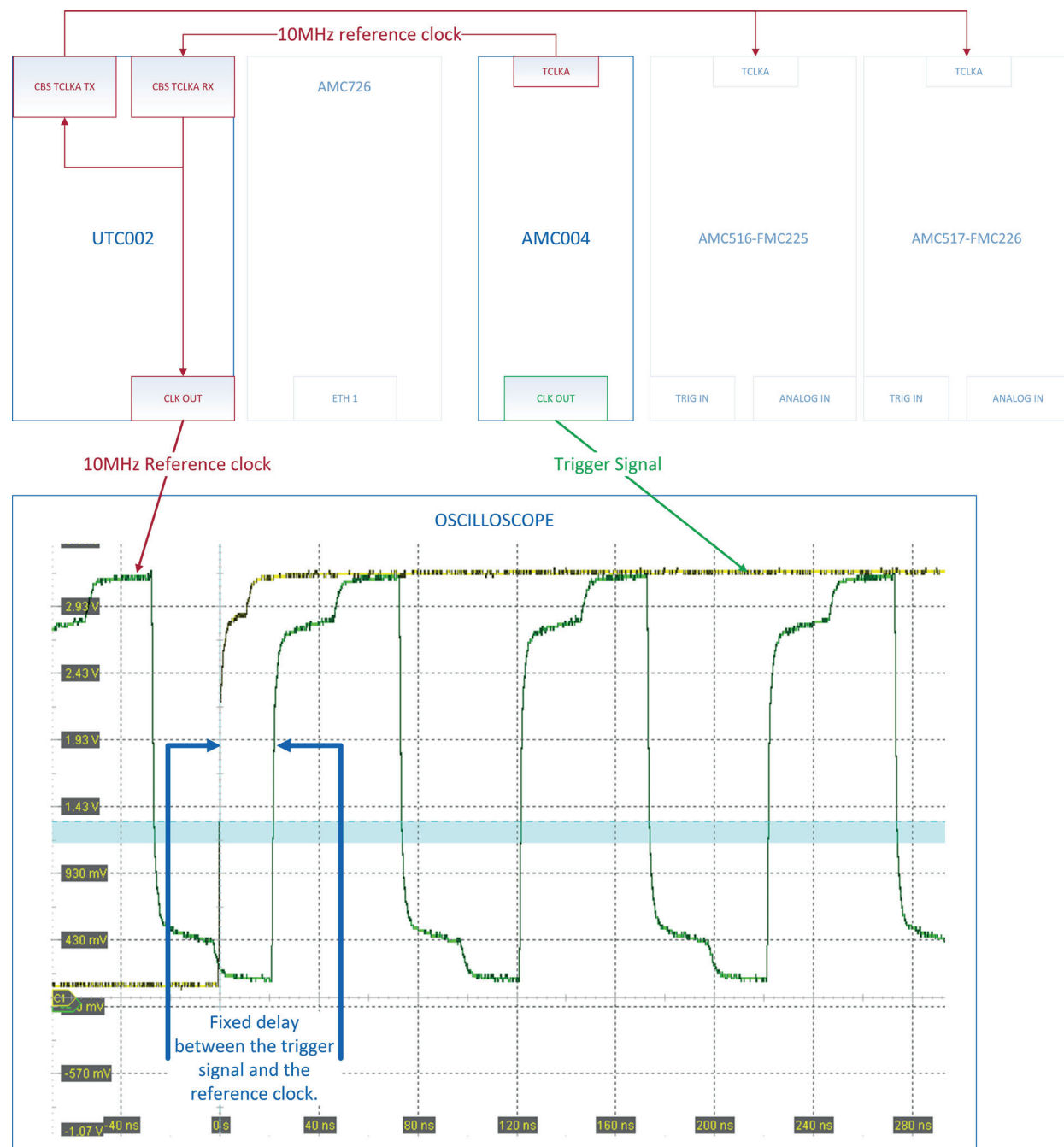

Figure 2: Deterministic delay between AMC004 trigger and 10MHz clock

The ADCs (ADC12J4000) on FMC225/FMC226 are configured with a 4x Digital Down Converter (DDC). The ADC's internal Direct Digital Synthesizer (DDS) center frequency can be configured from the DAQ Series™ GUI. The ADC output is a 15bit I/Q, 1GHz bandwidth DC-centered signal, transferred to the FPGA via the JESD204B protocol.
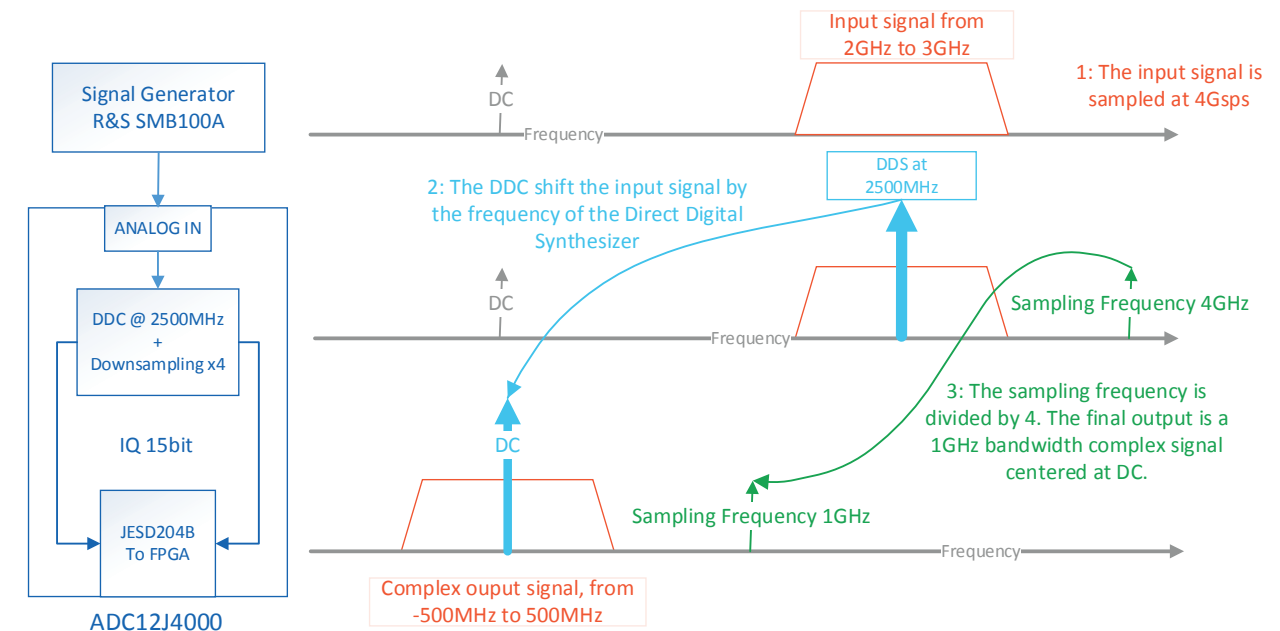

Figure 3: ADC12J4000 Digital Down Converter

Two instances of the DAQ Series™ IOC run in parallel on the AMC726, each providing the control/status/results interface to its respective DAQ AMC over PCIe.

The DAQ Graphical User Interface has been enhanced to allow connection to both DAQ Series IOC over the AMC726 front panel GbE. The main interface displays the Control and Status of AMC517-FMC226 and AMC516-FMC225. The Amplitude graph displays the I/Q of the current snapshot captured by AMC517-FMC226 and AMC516-FMC225, as well as the snapshot timestamp.
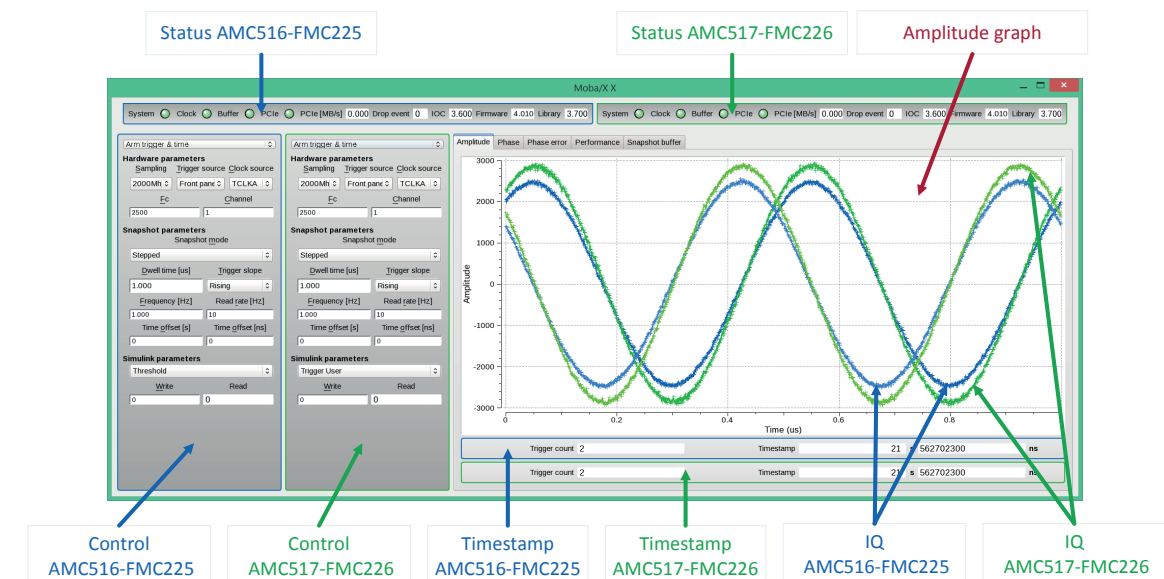

Figure 4: DAQ Series dual channel GUI

A phase computation is available on the DAQ Series™ IOC, linked to two types of phase plots in the DAQ Series™ GUI (Phase and Phase error). This allows the user to monitor the phase difference between AMC516-FMC225 and AMC517-FMC226 in real time.

The Phase figure displays the angle (in milli-radian) of the current snapshot captured by AMC517-FMC226 and AMC516-FMC225.

The Phase error figure displays, for each sample (t) of the current snapshot, a point with the coordinates {X = phase of sample (t) AMC516-FMC225, Y = phase of sample (t) AMC517-FMC226}. This plot provides a representation of the phase difference, as well as phase difference jitter.
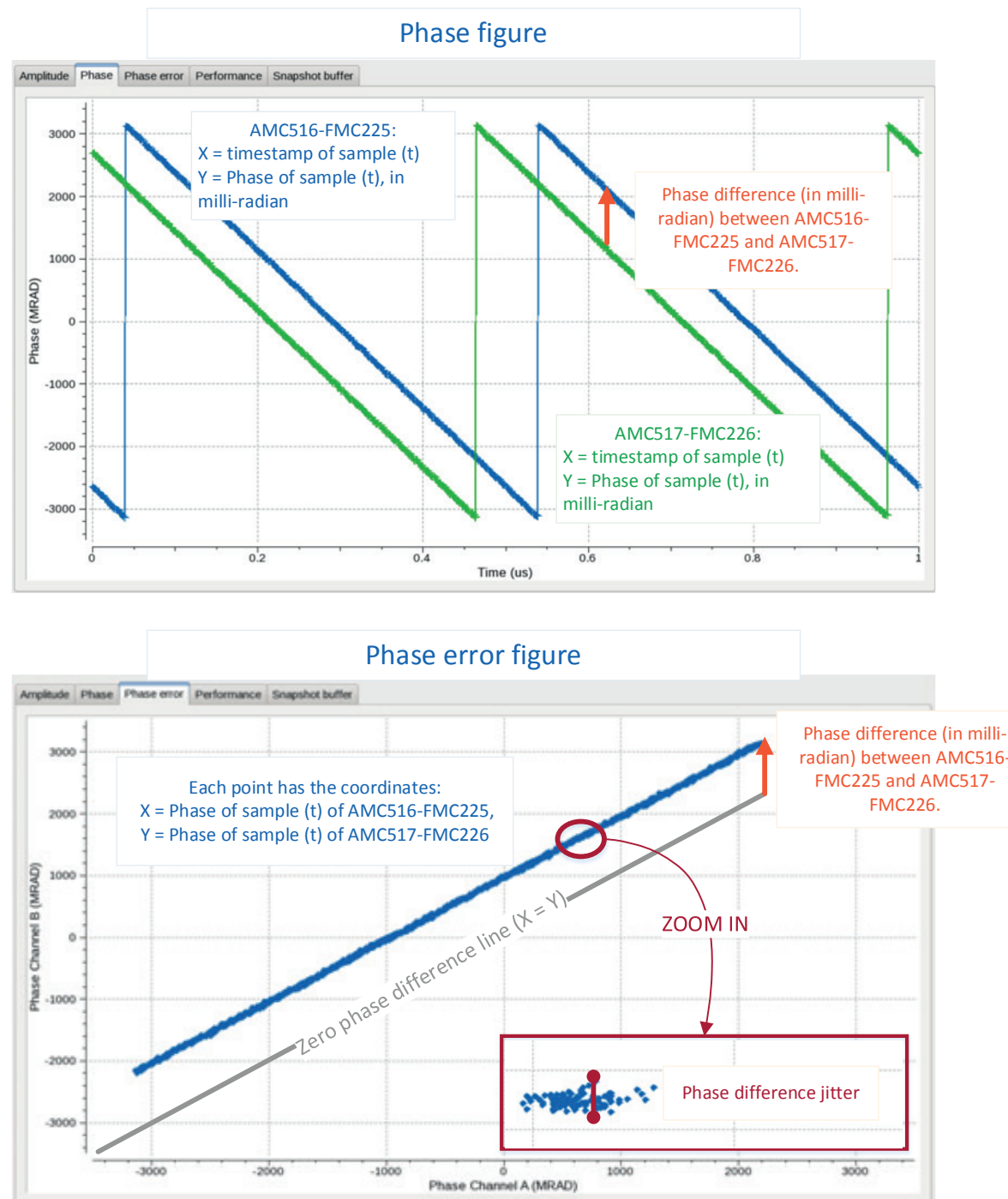
The phase difference (Delta Phase) between AMC516-FMC225 and AMC517-FMC226 has been measured for different input frequencies, and different DDC configurations. The phase difference is then converted to a sampling time difference (Delta sample).

DDC Center Frequency (MHz)	Input Frequency (MHz)	Delta Phase (mrad)	Delta Sample (ps)
1500	1302	184	22.5
1500	1502	183	19.4
1500	1802	101	8.9
2500	2302	-65	-4.5
2500	2502	71	4.5
2500	2800	44	2.5
3500	3302	-38	-1.8
3500	3502	-11	-0.5
3500	3802	13	0.5

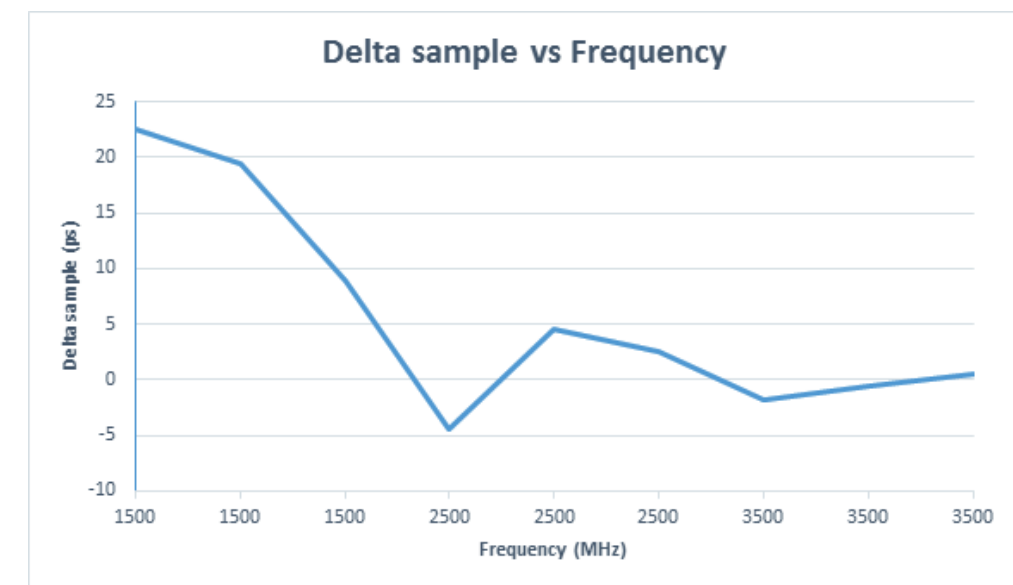Figure 5: DAQ Series Phase display

Figure 6: Result Delta sample vs Frequency

For more details on this application note please refer to our white paper available via www.vadatech.com. VadaTech is able to offer costed services to configure equipment as shown here. For more information please contact sales@vadatech.com

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