

# AMC573

Xilinx Zynq® UltraScale+ RFSoc  
FPGA, AMC



AMC573

## Key Features

- Xilinx Zynq® UltraScale+ RFSoc XCZU28DR FPGA
- 8 ADC/DAC to the front
- 8 GB of 64-bit wide DDR4 Memory (single bank) with ECC to CPU
- 8 GB of 64-bit wide DDR4 Memory (single bank to Fabric)
- MPSoC with block RAM and UltraRAM
- SD Card (option)
- 128 MB of boot Flash
- 64 GB of user Flash

## Benefits

- High density I/O all to front panel
- Zynq UltraScale+ MPSoC+ RF
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company



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# AMC573

The AMC573 utilizes the Xilinx XCZU28DR RFSoc and is compliant to AMC.1, AMC.2, AMC.3 and AMC.4 specifications. It has an onboard, re-configurable FPGA which interfaces directly to the AMC FCLKA, TCLKA-D. The module has two banks of 64-bit wide DDR4 memory with ECC (16 GB in total). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The front panel incorporates 18 HD RF Coaxial connectors routed to the 8 ADC (12-bit @ 4 GSPS) and 8 DAC (14-bit @ 6.4 GSPS) in the RFSoc. Also included are Trig-in, Trig-out, Clock inputs, dual USB, Dual Micro USB (RS-232) a DisplayPort interface and a dual High-density connector for external I/O. The default I/O is 8 LVDS or single ended +1.8V I/O but can be modified to meet customer requirements. Please contact VadaTech sales for details.

The XCZU28DR includes a quad-core ARM Cortex-A53 application processing unit and dual-core Cortex-R5 real-time processing as well as over 4,200 DSP, 930K logic cells and over 60 Mb of internal memory (including 22.5 Mb of UltraRAM). The chip also includes a soft-decision FEC block supporting low-density parity check (LDPC) decode/encode and Turbo decode for use in 5G wireless, backhaul, DOCSIS, and LTE applications.

The Module has onboard 64 GB of Flash, 128 MB of boot flash and an SD Card as an option.



Figure 1: AMC573



Figure 2: AMC573 Conduction Cooled

# Block Diagram

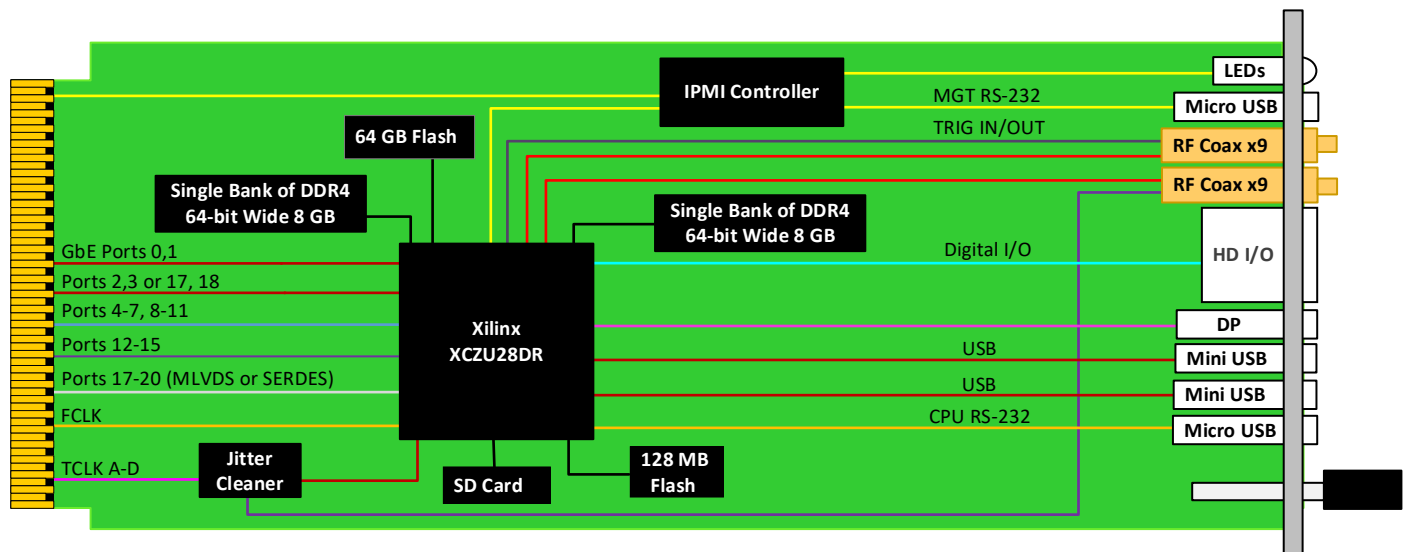


Figure 3: AMC573 Functional Block Diagram

# Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from customer support site along with the reference images.

## Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

[Xilinx Vivado Design Suite](#), [Xilinx System Generator for DSP](#).

# Specifications

Architecture		
Physical	Dimensions	Single module, mid-size (full-size optional)
		Width: 2.89" (73.5 mm)
		Depth 7.11" (180.6 mm)
Type	AMC FPGA Carrier	Xilinx Zynq® UltraScale+ RFSoc
Standards		
AMC	Type	AMC.0, AMC.1, AMC.2, AMC.3 and AMC.4
Module Management	IPMI	IPMI v2.0
GbE	Lanes	Port 0 and 1
PCIe	Lanes	x4 (Ports 4-7/8-11) or x8 (Ports 4-11) and additional Ports on 12-15
10GbE/40GbE/SRIO		Ports 4-7, 8-11 and additional Ports on 12-15
Configuration		
Power	AMC573	45W FPGA load dependent
	RTM	None
Environmental	Temperature	See <a href="#">Ordering Options</a> and <a href="#">Environmental Spec Sheet</a>
		Storage Temperature: -40° to +85°C
	Vibration	Operating 9.8 m/s <sup>2</sup> (1G), 5 to 500 Hz on each axis
	Shock	Operating 30G on each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	Interface Connectors	High-density multi-way RF Coaxial connectors x2
		Micro USB for RS-232 (Management and CPU)
		Dual Mini USB
		Display Port
		High Density I/O Connector
	LEDs	IPMI management control
		Debug (user defined) LED
	Mechanical	Hot-swap ejector handle
Software Support	Operating System	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see <a href="#">VadaTech Terms and Conditions</a>	

## INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

# Ordering Options

## AMC573 – ABC-DEF-GHJ-KL0

<b>A = Ports 12-15 to FPGA</b> 0 = Not routed 1 = Routed as SERDES*	<b>D = SD Card</b> 0 = No SD Card 1 = SD Card (32 GB)	<b>G = Clock Holdover Stability</b> 0 = Standard (XO) 1 = Stratum-3 (TCXO)
<b>B = Ports 17-20 as LVDS or SERDES</b> 0 = Not routed 1 = LVDS 2 = SERDES**	<b>E = FPGA Speed</b> 1 = Low 2 = High 3 = Reserved	<b>H = I/O</b> 0 = 8 LVDS or singled ended I/O at +1.8V 1 = Reserved 2 = Reserved 3 = Reserved
<b>C = Front Panel</b> 1 = Reserved 2 = Mid-size 3 = Full-size 4 = Reserved 5 = Mid-size, MTCA.1 (captive screw) 6 = Full-size, MTCA.1 (captive screw)	<b>F = PCIe Fabric</b> 0 = No PCIe 1 = PCIe on Ports 4-7 2 = PCIe on Ports 8-11 3 = PCIe on Ports 4-11	<b>J = Temperature Range and Coating</b> 0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane*** 7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic***
<b>K = RF Input/Output†</b> 0 = 1GHz ~ 4GHz (Balun Anaren) 1 = 10MHz ~ 4GHz (Mini Circuit) 2 = Reserved 3 = Reserved	<b>L = Back plane CLK A/B</b> 0 = Thru the CBS (Cross Bar Switch) 1 = By-pass mode	

Notes: \* These ports are not LVDS compatible.

\*\* SERDES ports 2/3 are route to ports 17/18 and two additional SERDES are routed to ports 19/20

\*\*\* Conduction cooled; temperature is at edge of module. Consult factory for availability. †The performs is based on the Balun selection, contact VadaTech for other options.

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

## Related Products

VT951



- MicroTCA rugged 1U 19" rackmount chassis platform
- Designed to meet MIL-STD-810F, MIL-STD-901D for shock/vibration
- Supports up to six single module mid-size

AMC592



- AMC FPGA carrier for FMC per VITA 57
- Xilinx UltraScale™ XCKU115 FPGA
- Supported by DAQ Series™ data acquisition software

FMC214



- Dual complete transceiver signal chain solution using Analog Devices AD9361 transceiver
- Frequency range 70 MHz to 6 GHz with instantaneous bandwidth from 200 kHz to 56 MHz
- MIMO transceiver is Time Domain Duplex (TDD)

# Contact

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