PCI536

PCIe FPGA Carrier for FMC+, Altera Arria-10 GX1150

PCI536

Key Features

- PCIe FPGA carrier for FMC+ per VITA 57
- Altera Arria-10 GX1150 in F1517 package
- Clock jitter cleaner
- 16 GB of DDR4 (2 bank of 64-bits)
- Active cooling for FPGA and FMC
- Dual x6 dedicated private channels for intra-board communication via the back

Benefits

- Arria-10 FPGA in F1517 package
- Two Bank of 64-bit wide DDR4 memory allows larger buffer sizes while processing and queuing data to the host
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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The PCI536 is based on the Altera Arria-10™ GX1150 FPGA in F1517 package. The FPGA interfaces directly to the FMC+ DP 0-23 (single connector) and all FMC+ LA/HA/HB pairs, making it compatible with a wide range of industry standard VITA 57 modules. The PCI536 has x8 PCIe edge connector routed to the FPGA PCIe Gen3 hard IP block. It also has interface to two DDR4, 64-bit wide, with 16 GB total memory. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The Module has dedicated dual x6 link that can interconnect to other modules through the back as private channels.

See Intel FPGA Solutions for the advantages of using VadaTech products during application development.
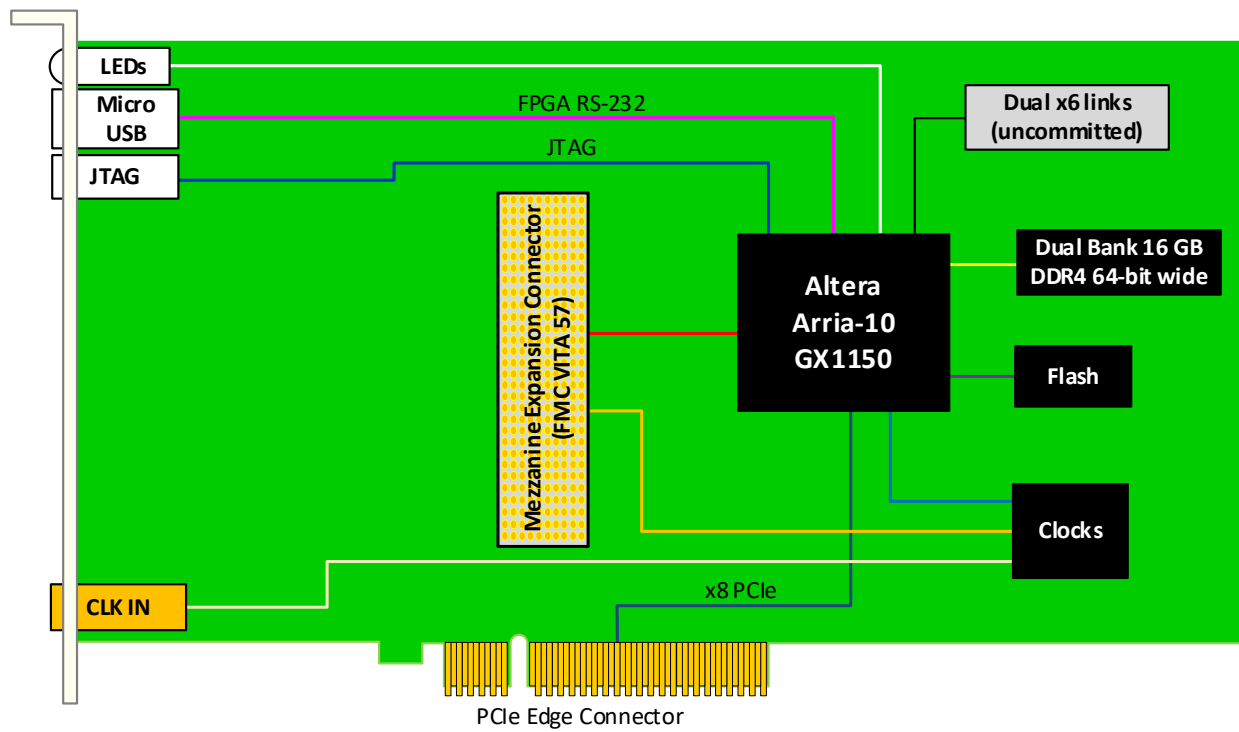

Figure 1: PCI536

Block Diagram

Figure 2: PCI536 Functional Block Diagram

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

[Xilinx Vivado Design Suite](), [Xilinx System Generator for DSP]().

Compatible FMC+

VadaTech offers VITA 57 compatible FMCs providing ADC, DAC, RF transceivers and network interfaces. These FMCs are widely deployed in commercial and mil/aero form factors. Please contact VadaTech Sales for more information.

Specifications

Architecture		
Physical	**Dimensions**	Single Module
		Width: 4.36" (110.74 mm)
		Depth: 10.32" (311.98 mm)
Type	**PCI Carrier**	PCI FPGA Carrier for FMC+
Standards		
PCIe	**Lanes**	PCIe Gen3 x8
Configuration		
Power	**PCI536**	~30W application dependent
Environmental	**Temperature**	See Ordering Options
		Storage Temperature: –40° to +85°C
	Vibration	Operating 9.8 m/s^2 (1G), 5 to 500 Hz on each axis
	Shock	30Gs on each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	**Interface Connectors**	Front panel FMC+
		FPGA RS-232 via micro USB
		CLK IN from SSMC
	LEDs	Four User defined
Software Support	**Operating System**	Agnostic
Other		
MTBF		MIL Hand book 217-F@ TBD hrs
Certifications		Designed to meet FCC, CE and UL certifications, where applicable
Standards		VadaTech is certified to both the ISO9001:2015 and AS9100D standards
Warranty		Two (2) years, see VadaTech Terms and Conditions

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

PCI536 – 000-0E0-G0J

		G = Clock Holdover Stability
		0 = Standard (XO) 1 = Stratum-3 (TCXO)
	E = FPGA Speed	
	1 = Highest 2 = High 3 = Reserved	
		J = Temperature Range and Coating
		0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane 7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic

Notes:
For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.
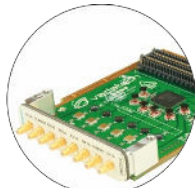
Related Products

AMC536

- Single module, mid-size AMC (full-size optional)
- Altera Arria-10 GX1150 in F1517 package
- AMC Ports 4-11 are routed to FPGA per AMC.1, AMC.2 and AMC.4

FMC214

- Dual complete transceiver signal chain solution using Analog Devices AD9361 transceiver
- Frequency range 70 MHz to 6 GHz with instantaneous bandwidth from 200 kHz to 56 MHz
- MIMO transceiver is Time Domain Duplex (TDD) and Frequency Domain Duplex (FDD) compatible

FMC223

- Single module DAC 14-bit @ 2.5 GSPS (AD9739)
- 2 Vpp differential Analog output swing
- Programmable DSP clock

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014

Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan

Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR

Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

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