VPX005

3U OpenVPX Switch, 1/10/40GbE with Integrated Health Management and Clocking

VPX005

Key Features

- Unified 1 GHz quad-core CPU for, Shelf Manager, and Fabric management
- Automatic fail-over with redundant VPX005
- Dual 100/1000/10G uplink on the front panel
- Full Layer 3 managed Ethernet switches
- Non-blocking 1/10/40GbE
- PLL synthesizer for generating any clock frequency disciplined to GPS/SyncE/IEEE1588
- VITA 46, VITA 48, VITA 65 compliant

Benefits

- Sophisticated clocking features enabling GPS/IEEE1588/SyncE/NTP Grand Master Clock
- Optional virtual JTAG capability for remote programming and debugging eases FPGA code development
- VadaTech's Scorpionware® Shelf Management Software included at no additional cost
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™

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VPX005

The VadaTech 3U VPX005 switch with integrated health management, is the most feature-rich and powerful 40G switch on the market. The management software is based on VadaTech's robust Carrier Manager and Shelf Manager which have been tested, approved and deployed for years by our Customers.

The Shelf Manager in the quad-core CPU manages the Power Modules, Cooling Units, and the VPX payloads modules within the chassis per VITA46.11 with Tier1 and Tier2 capability. It also manages the 40GbE switch.

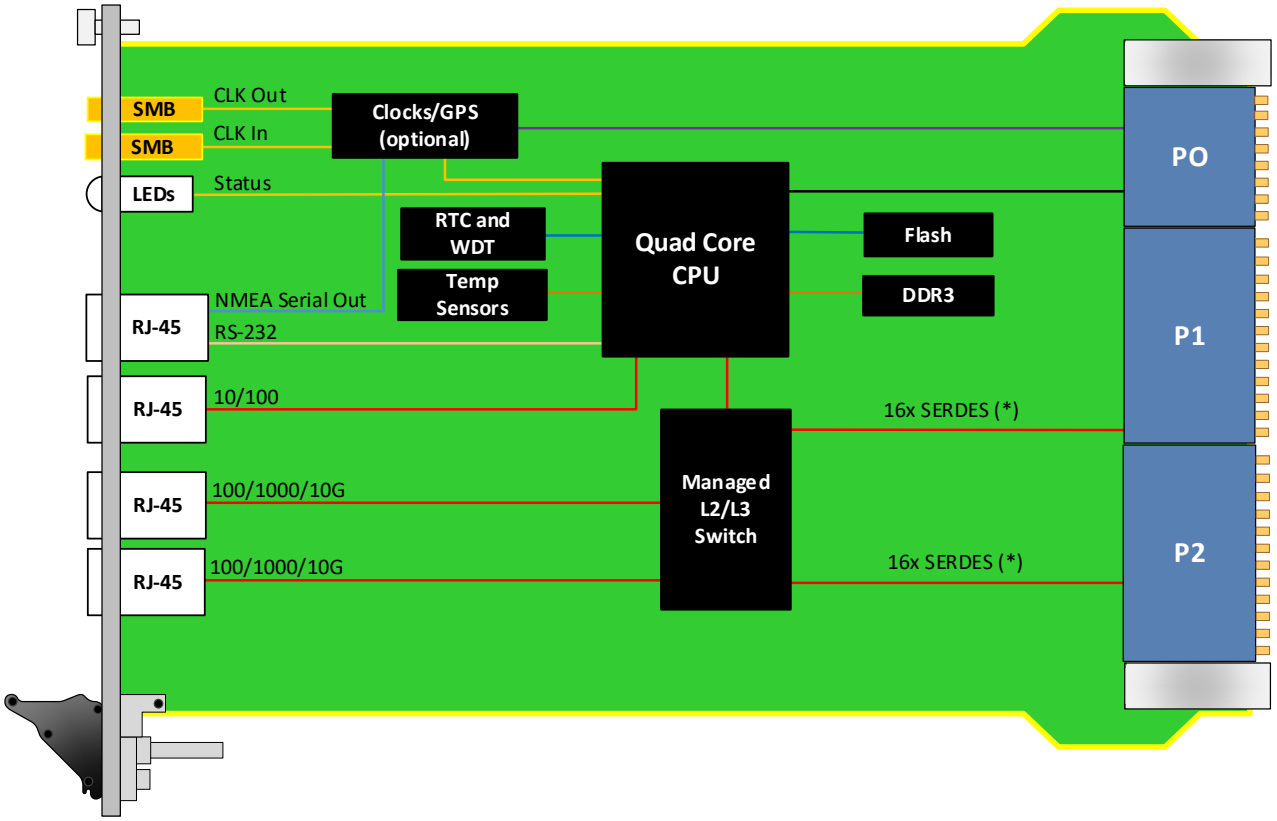
The 40G Ethernet switch is managed with an enterprise grade Layer 2/3 switching/routing stack which also supports Synchronous Ethernet (SyncE).

The x16 SERDES can be configured as mix of 40G-KR, 10G-KR, 10G-XAUI and/or GbE.

The unit runs Linux on its centralized quad-core CPU and has redundancy capability when used in conjunction with a second instance of the module. The firmware is HPM.2 compliant which allows for easy upgrades.

VPX005 provides ordering options for JTAG over Ethernet when used in conjunction with a JTAG Switch Module (JSM) in the chassis, and has ordering options for advanced clocking features including GPS or grand master clock and high-quality clock distribution/synthesis.

Block Diagram



* SERDES can be configured as mixed of 40G-KR (up to 4x40G on each P1/P2), 10G-KR (up to 16x on each P1/P2), 10-XAUI, and 1G (up to 16x on each P1/P2)

Figure 1: VPX005 Functional Block Diagram

Front Panel

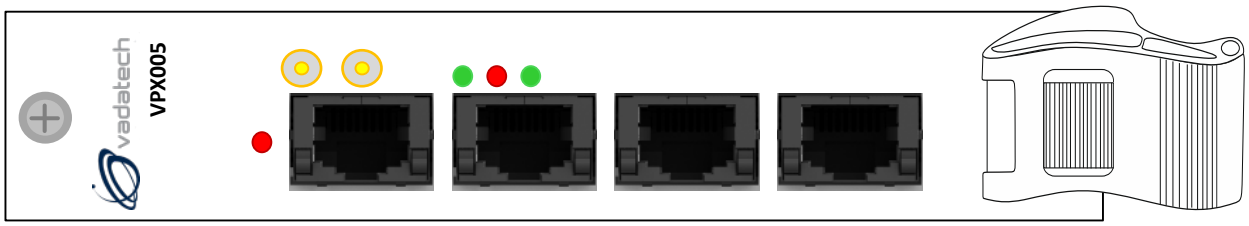


Figure 2: VPX005 Front Panel (per ordering options)

Architecture

IPMI Carrier Manager, Shelf Manager and Protocol Analyzer

The VPX005 utilizes the same proven standards-compliant IPMI management stack that has been utilized successfully in our previous generation products. It supports carrier manager, shelf manager, and protocol analyzer operations to help facilitate a seamless chassis integration experience. The IPMI stack enables a rich feature set including:

- IPMI v2.0 with IPMI v1.5 compatibility
- SDR, FRU, and SEL storage interfaces (SEL stored in MRAM for high-speed/non-volatile/no-wear-out access)
- Intelligent temperature, voltage, and current sensing
- Shelf cooling policy
- Shelf activation and power management/Automatic fail-over/redundancy management
- Alarm controls
- Event notification and flexible alerting policies
- CLI, SNMP, RMCP+, HTTP, and HPI
- IPMB Protocol Analyzer GUI for use on PC
- ScorpionWare GUI system manager integration tool on PC available separately

Base Channel Ethernet Switch

The VPX005 powerful 40G/10G/GbE switch s switch provides:

- Full Layer 2 or 3 management enabling enterprise-grade switching and routing
- Supports Synchronous Ethernet (SyncE) and IEEE1588 to facilitate advanced system synchronization via Ethernet
- 320 Gbps aggregate bandwidth for mixed 1GbE/10GbE/40GbE on SERDES lanes to P1 and P2

GPS and General Purpose Clocks

The VadaTech VPX005 has ordering option to include the most sophisticated clocking distribution in the market to meet the most stringent requirements such as high speed A/D, synchronization, timestamping, triggering, etc.... The VPX005 supports flexible front panel clock IO and functions port per ordering options G and can be ordered with a GPS receiver option. The receiver disciplines an onboard high-quality DPLL which is phase/frequency aligned to the atomic clocks in the GPS satellite constellation. The onboard clock synthesis/jitter cleaning capability can be utilized to convert this frequency into any frequency desired while still remaining locked to the GPS atomic clocks.

When the GPS Receiver option is purchased the VPX005 has the capability to re-transmit the incoming GPS data via Ethernet to other network nodes in the Trimble TSIP binary protocol format. This GPS data is also sent out the front panel GPS RS-232 serial port in the standard NMEA format for use by external equipment. It also supports general-purpose clocking features:

- Open VPX-compliant low-jitter/low-skew backplane routing
- Clock disciplining with arbitrary clock frequency output and holdover (Stratum-3 option) including 1PPS regeneration and holdover
- Flexible integration and synchronization between GPS, IEEE1588/SyncE, and NTP clocking enabling Grand Master clock functionality
- Any Frequency' high-quality clock generation/jitter cleaning for up to two user clocks
- Supports hitless automatic clock failover for improved reliability
- Optional built-in GPS receiver enables direct time/clock synchronization to the GPS satellite constellation

IEEE1588 PTP and NTP Grand Master Clock

The VPX005 can provide Ethernet time services to the chassis networks on the SERDES. It can be subordinate to an external PTP or NTP master server or when the GPS receiver option is purchased can act as a Grand Master clock utilizing the precision timing information provided via the GPS receiver and onboard disciplined oscillator.

Synchronous Ethernet

The VPX005 provides a Synchronous Ethernet (SyncE) on the 1G/10/40GbE fabric ports. With this feature, ports on the Ethernet switch can be designated as master or slave ports and the Ethernet fabrics within the chassis can be synchronized from end-to-end with external equipment. This feature utilizes advanced telecom-grade network synchronization PLLs to provide exceptional SyncE performance.

JTAG Master/JTAG via Ethernet Virtual Probe

The VPX005 ordering option F provide JTAG Master Capability to send out the configuration data streams via the network and chassis JTAG Switch Module (JSM) to configure arbitrary JTAG Slave devices on VPX cards. Virtual Probe services are also available to provide JTAG via Ethernet for Xilinx FPGAs. This allows for standard development tools such as Xilinx iMPACT/ChipScope to treat the switch/JSM combination as if it was a standard JTAG probe. This approach frees the developer from having to attach JTAG probes directly to the VPX or JSM which can be difficult when systems are already fully assembled. It also allows for remote debugging across long distances when required without the need to install additional JTAG equipment on-site. This option shall be selected in conjunction with JSM on the chassis (contact Sales for details).

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
Type	**Controller**	OpenVPX Switch with Integrated Health Management
Standards		
VPX	**Type**	VITA 46, VITA 48.1 per option G
VPX	**Type**	VITA 65 OpenVPX
Module Management	**IPMI**	IPMI v2.0
		HPM v1.0
Configuration		
Power	**VPX005**	Option load dependent (typical 35W)
		On P0; VS1 = 12V
Front Panel	**Interface Connectors**	100/1000/10G from L2/L3 Base Switch Fabric (x 2 RJ-45) for H=0/1
		CPU 10/100 (RJ-45) for H=0/1
		CPU RS-232 (RJ-45) for H=0/1
		Option for GPS NMEA serial data in/out (RJ-45) for H=0/1
		LEDs Status
		Two CLK IN/OUT (SMB); CLK IN becomes GPS ANT IN with GPS receiver option D
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	CPU on P0
		Clocks/GPS (Optional) on P0
		1GBASE-KR/10GBASE-KR/40GBASE-KR4 and 10G-XAUI on P1/P2
		CPU RS-232 to P1; CPU 10/100 to P2; no front IO for H=2/3/4
Software Support	**Operating System**	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX005 – A0C-DEF-GHJ

A = VPX Connector Type	D = Front Panel Clocking	G = Applicable Slot Profile
0 = Standard 50u Gold Rugged 1 = KVPX Connectors	0 = No Clocking 1 = Dual LVCMOS Clock In/Out 2 = Sine Wave In + LVCMOS In/Out 3 = Built-in GPS receiver + LVCMOS In/Out 4 = Dual Sine Wave In 5 = GPS receiver + Sine Wave In 6 = Sine Wave In (up to 17dBm) +TTL/LVCMOS In	0 = 5 HP, VITA 46 (IEEE1101.1) 1 = 5 HP, VITA 48.1
	E = Clock Holdover Stability	**H = Environmental**
	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification
C = 40GbE Switch Aggregate Bandwidth	**F = JTAG Virtual Probe**	**J = Conformal Coating**
1 = 320 Gbps 2 = Reserved	0 = No JTAG Virtual Probe 1 = JTAG Virtual Probe	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes:

* Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX516

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX518

- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Zynq-7000 FPGA in FFG-900 package (XC7Z100 or XC7Z045)
- High-performance clock jitter cleaner

VPX599

- 3U FPGA Dual DAC and dual ADC per VITA 46
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014
Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan
Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR
Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

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DOC NO. 4FM737-12 REV 01 | VERSION 1.9 – NOV/21