VPX529

Dual DAC, 14-bit @ 5.7 GSPS, Virtex-7, 3U VPX

Key Features

- 3U Dual DAC 14-bit @ 5.7 GSPS (AD9129) (2.85 GSPS direct RF synthesis)
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- Internal or external clock with an onboard wideband PLL and clock jitter cleaner
- Protocols such as PCIe, SRIO, 10GbE/40GbE, etc. are FPGA programmable
- Triple bank QDR2+ (432 Mb total) and 1 GB DDR3
- Optional connections on P2
- Health Management through dedicated Processor

Benefits

- Reference design with VHDL source code speeds application development
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX529

The VPX529 provides two Analog Devices (AD9129). Each chip core is based on a quad switch architecture that enables dual-edge clocking operation, effectively increasing the DAC update rate to 5.7 GSPS when configured for Mix-Mode™ or 2x interpolation.

The high dynamic range and bandwidth enable multi-carrier generation up to 4.2 GHz. The onboard Virtex-7 690T provides signal processing capability for complex waveform generation, appropriate for applications such as SDR, ATE and jamming.

Additional ports are optionally routed to the FPGA from P2, providing the user with flexibility to support custom high-bandwidth interconnects between compatible FPGA modules (depending on backplane capabilities).

The FPGA is supported by Flash memory for boot image storage, three banks of QDR-II+ for fast data buffering and a further bank of DDR3 for local data.

The module includes a very flexible clocking sub-system, supporting internal or external (backplane or FMC connector) clock source with internal PLL/jitter cleaner.

The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

Block Diagram

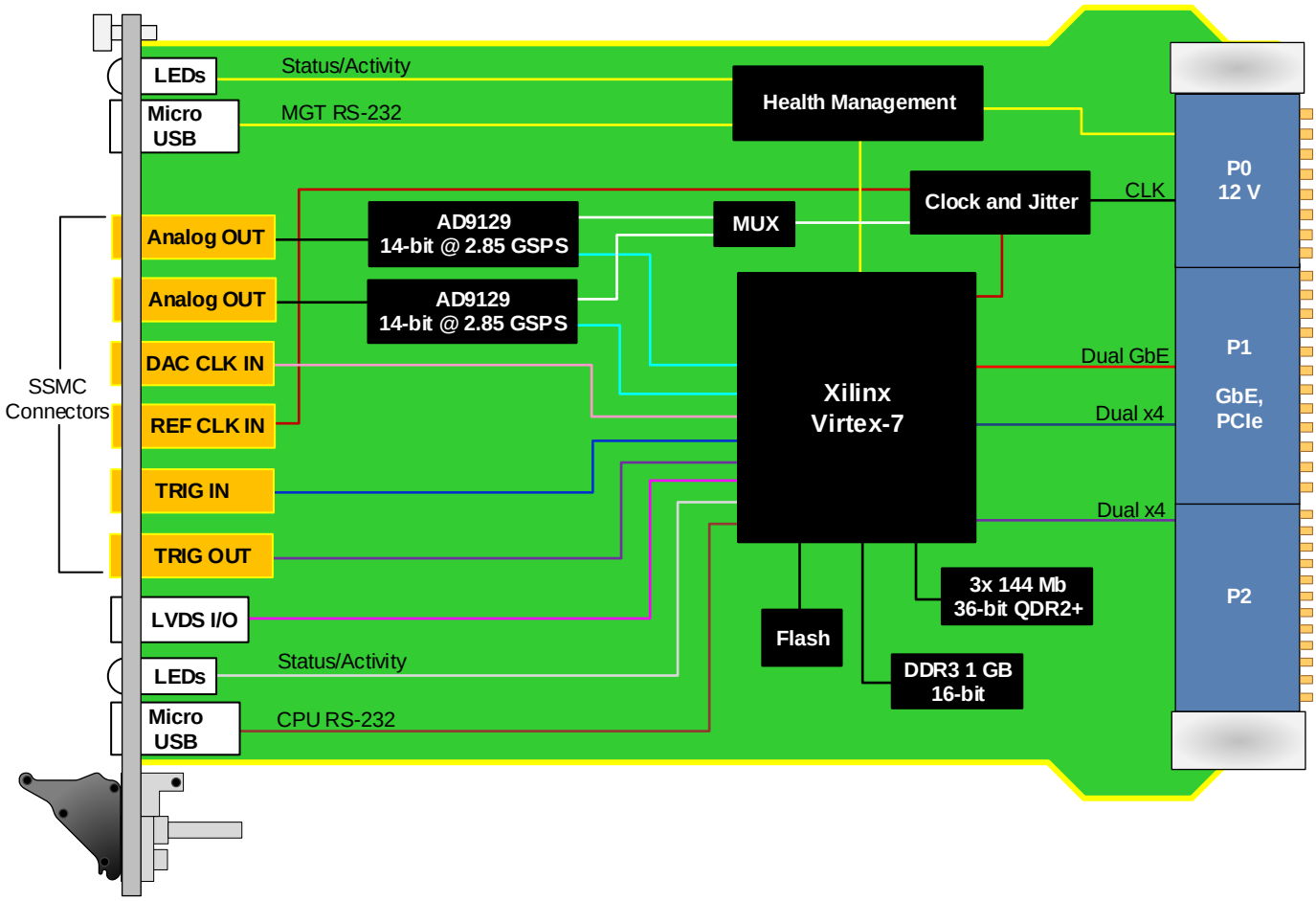

Figure 1: VPX529 Functional Block Diagram (Air Cooled Version)

Front panel

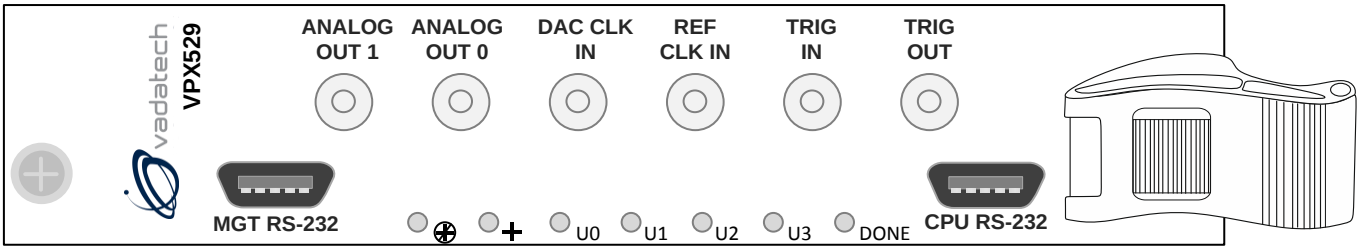

Figure 2: VPX529 Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
Configuration		
Power	**VPX529**	TBD (dependent on FPGA load and FMC)
	FPGA	Xilinx Virtex-7 (XC7VX690T)
	Memory	432 Mb QDDR2+ (3 x 36-bit) and 1 GB DDR3 (16-bit)
Front Panel	**SSMC**	Dual ADC, CLK IN, TRIG IN
	Display Port	LVDS I/O
	Micro USB	RS-232 from FPGA and RS-232 from Health Management
	LEDs	User defined by the FPGA and Health Management
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	Dual x4 fabric on P1 (PCIe Gen3/10GbE/40GbE/SRIO per FPGA load)
		Dual GbE on P1
		Dual x4 fabric on P2 (optional)
	Power Supplies	On P0: VS1 = 12V
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX529 – ABC-DEF-GHJ

A = RF Clock Sampling	D = FPGA Speed	G = Applicable Slot Profiles
0 = Front Panel (with XO hold-over) 1 = Onboard Wideband PLL (with XO hold-over) 2 = Front Panel (with TCXO hold-over) 3 = Onboard Wideband PLL (with TCXO hold-over)	0 = Reserved 1 = High 2 = Highest	0 = 5 HP
B = Expansion Plane (P2)	**E = VPX Connector Type**	**H = Environmental**
0 = No Expansion Plane 1 = Expansion Plane Routed	0 = Standard 50u Gold Rugged 1 = KVPX Connectors	See Environmental Specification
C = FPGA	**F = PCIe Option (P1) for Data Port 1/2**	**J = Conformal Coating**
0 = Reserved 1 = Reserved 2 = XC7VX690T	0 = No PCIe 1 = PCIe/None 2 = None/PCIe 3 = PCIe/PCIe	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX004

- Unified 1 GHz quad-core CPU for, Shelf Manager, and Fabric management
- 1GbE base switch with dual 100/1000/10G uplink
- Full Layer 3 managed Ethernet switch

VPX754

- 3U VPX module Intel 5th Generation Xeon D-1577, D-1548 or D-1520 (Broadwell) SoC
- PCIe Gen3 dual x4 or single x8
- Front-panel video out via micro HDMI

VTX870

- Open VPX benchtop development platform
- Up to five 3U VPX payload slots
- Compatible with 0.8-inch, 0.85-inch and 1.0-inch modules

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