VPX552

Xilinx Kintex UltraScale™ with Intel® Xeon™ SoC, 6U VPX

VPX552

Key Features

- Intel Broadwell-D integrated with Xilinx Kintex UltraScale™ XCKU115 FPGA
- Intel® 5th Generation Xeon System-on-Chip (SoC)
- CPU 32 GB of DDR4 with ECC
- FPGA 16 GB of DDR4
- XMC site
- VITA66.5 for optical to rear
- Health Management through dedicated Processor

Benefits

- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™

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VPX552

The VPX552 is a 6U VPX board with Kintex UltraScale™ FPGA and Intel® 5th generation Xeon 4-core, 8-core or 16-core Processor (Broadwell-D).

The efficient SoC design has low power consumption and integrated PCH technology. The processor has 32 GB of dual-bank DDR4 memory with ECC and Flash for the OS with Trusted Platform Management (TPM). The VPX552 has four 10GbE route to the rear via VITA 66.5 optical.

The BIOS allows booting from onboard Flash (SATA) or PXE boot of the OS via any of its Ethernet Ports.

The onboard FPGA is a Kintex UltraScale™ with 16 GB of dual-bank DDR4 Memory. High speed SERDES are routed to the rear (copper via P1 and P2, optical via VITA 66.5). GPIO signals are routed to the rear as LVDS and M-LVDS.

An XMC site is supported by PCIe x8 and has I/O routed to the rear per VITA 46.9 as xD12.

The health management is based on the VITA 46.11.

The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

Please contact VadaTech for details of Conduction Cooled versions.

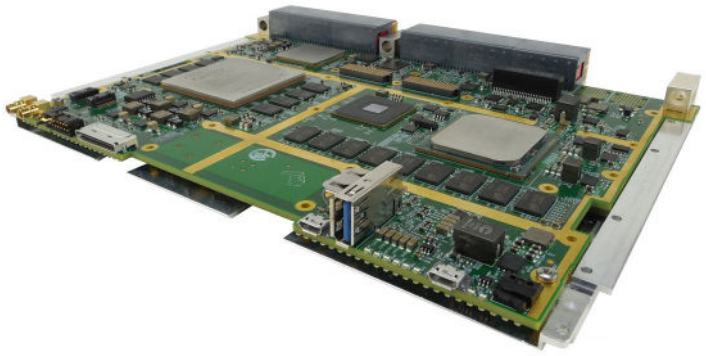

Figure 1: VPX552

Figure 2: VPX552 Conduction Cooled

Block Diagram

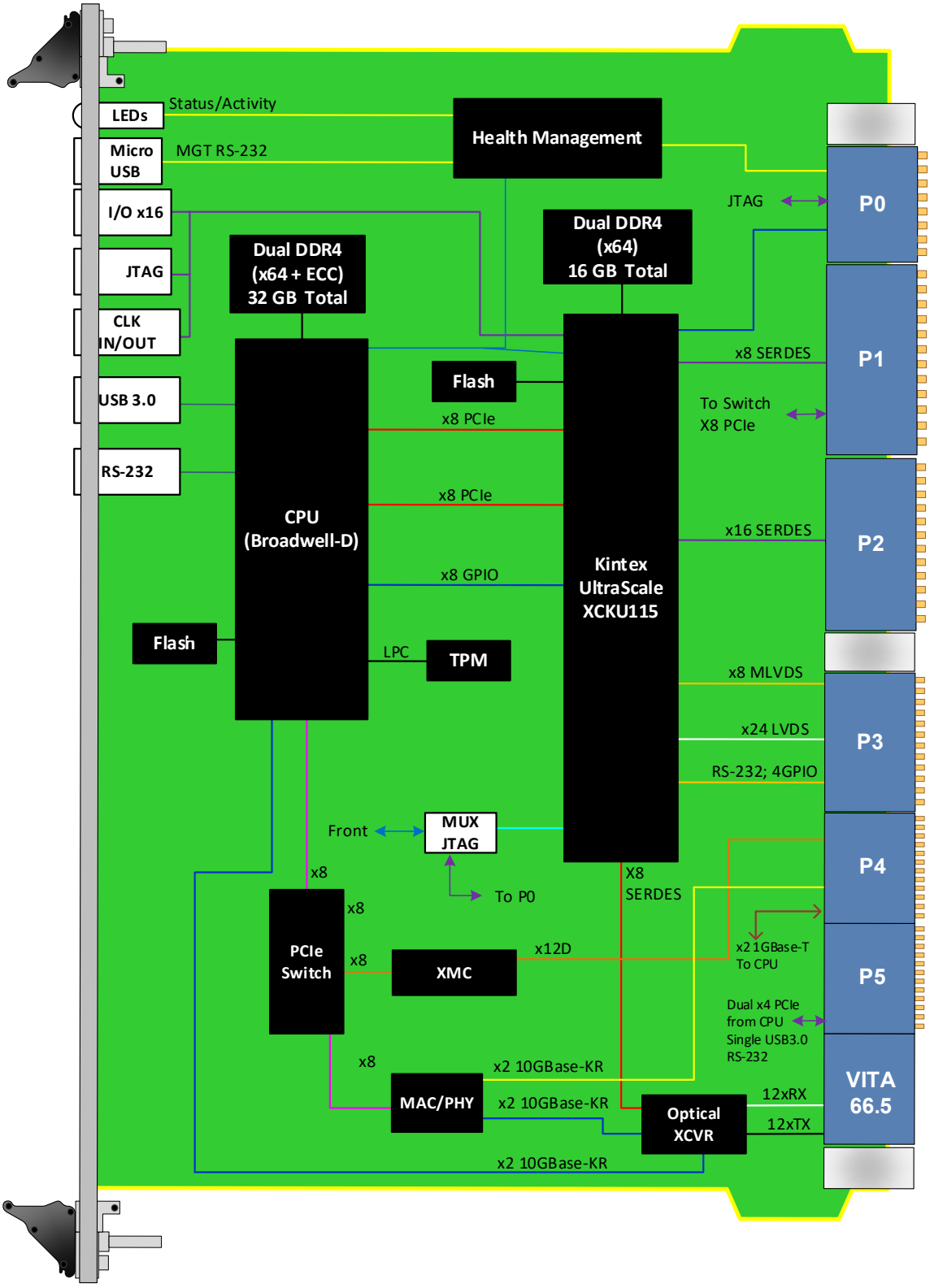

Figure 3: VPX552 Functional Block Diagram

Backplane Pinout

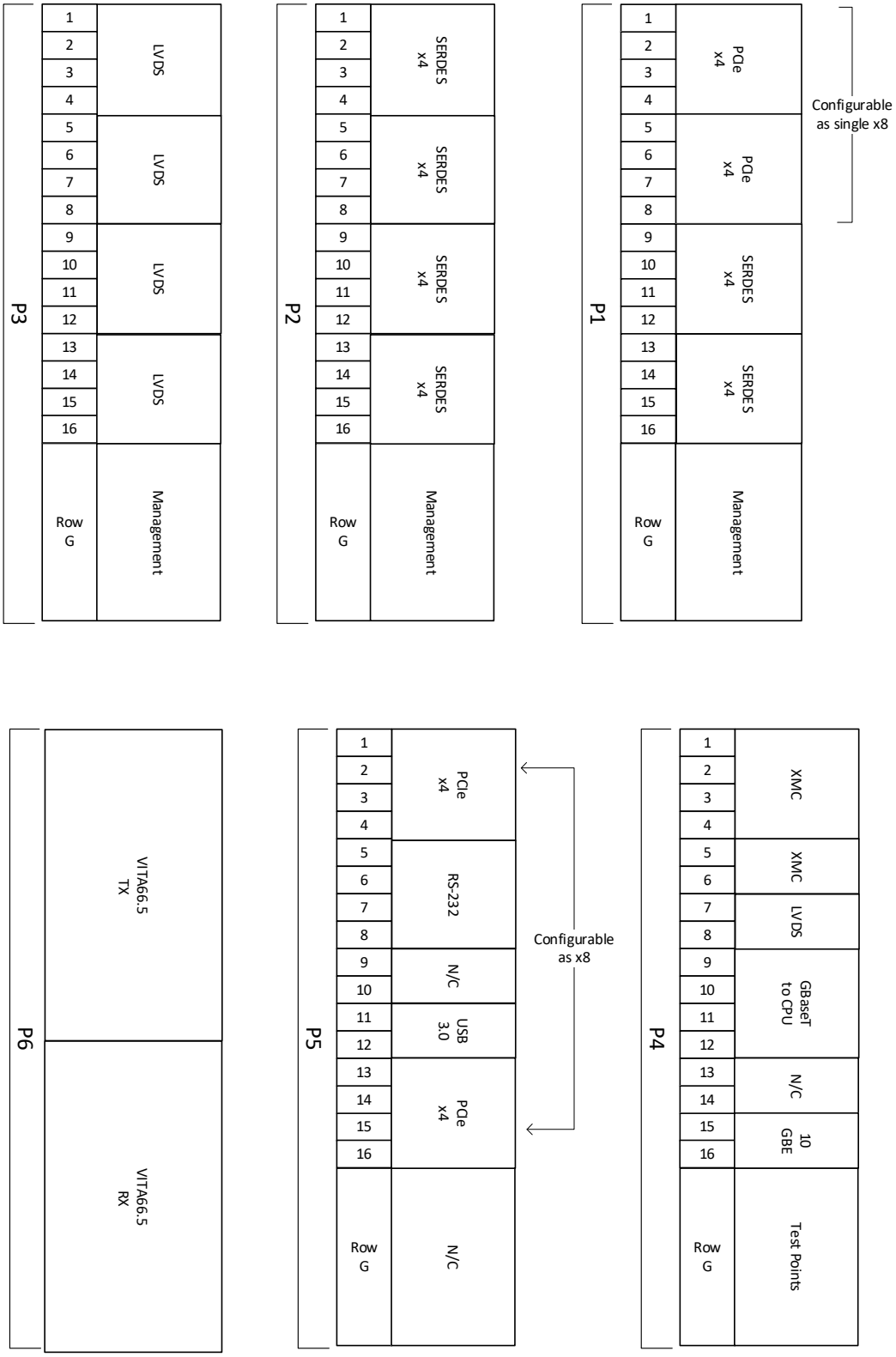

Figure 4: VPX552 Backplane Pinout

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	6U, VPX
FPGA		Xilinx Kintex UltraScale™ XCKU115, 16 GB DDR4
Configuration		
Power	**VPX552**	~80W (CPU and FPGA load dependent)
Front Panel	**JTAG**	Standard JTAG header via front or P0
	Micro USB	RS-232 from Health Management
	LEDs	User defined by the FPGA and Health Management
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	P1: x8 SERDES and x8 PCIe
		P2: x16 SERDES
		P3: x8 MLVDS, x24 LVDS, GPIO and RS232 from FPGA
		P4: x12D Mapping, x2 1GBase-T and x2 10GBase-KR
		P5: CPU I/O including Dual PCIe x4, USB3.0 and RS232
		P6 location: VITA66.5 12 x TX/RX
Software Support	**Operating System**	Linux, VxWorks and/or Windows
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX552 – ABC-DE0-GHJ

A = Processor	D = FPGA Speed	G = Applicable Slot Profiles
0 = 4C, 2.2 GHz, 6 MB LLC, Xeon D-1527 1 = Reserved 2 = 8C, 2 GHz, 12 MB LLC, Xeon D-1548 3 = 16C, 1.3 GHz, 24 MB LLC, Xeon D-1577 4 = 8C, 1.6 GHz, 12 MB LLC, Xeon D-1539 5 = Reserved	1 = Reserved 2 = High 3 = Highest	0 = 5 HP, VITA 48.1 1 = 10 HP, VITA 48.1
B = SATA	**E = XMC Connectors**	**H = Environmental**
0 = No SATA 1 = 64 GB	0 = VITA 42 1 = VITA 61	See Environmental Specification
C = VPX Connector Type		**J = Conformal Coating**
0 = Standard 50u Gold Rugged 1 = KVPX Connectors		0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Notes:

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

Air Cooled			Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes:

*Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX516

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX592

- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

Contact

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