VPX580

Zynq UltraScale+ FPGA, Dual FMC Carrier, 6U VPX

VPX580

Key Features

- Xilinx UltraScale+ XCZU19EG FPGA
- 8 GB of 64-bit wide DDR4 Memory (single bank) with ECC
- Dual FMC+ sites (16 SERDES to each) on a 6U VPX
- MPSoC with block RAM and UltraRAM
- Health Management through dedicated Processor

Benefits

- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX580

The VPX580 is a 6U VPX FPGA Carrier based on Xilinx UltraScale+ XCZU19EG MPSoC FPGA with dual FMC+ sites. The unit has an onboard, re-configurable FPGA which interfaces directly to the VPX P1-P2 connectors, FMC+ DP0-15 and all FMC LA/HA/HB pairs. Each FMC+ site has 16 SERDES routed from the FPGA and each site is supported by an Interlaken hardcore processor.

The FPGA has interface to a single DDR4 memory channel (64-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host. The module has onboard 64 GB of Flash, 128 MB of Boot Flash and an SD Card option.

The XCZU19EG FPGA has 1968 DSP Slices and 1143K logic cells. The XCZU19EG includes a quad-core ARM processor. Dual GbE from P1 is 1000-BaseBX to the ARM processor.

Onboard microcontroller implements Tier 2 health management.

Figure 1: VPX580

Block Diagram

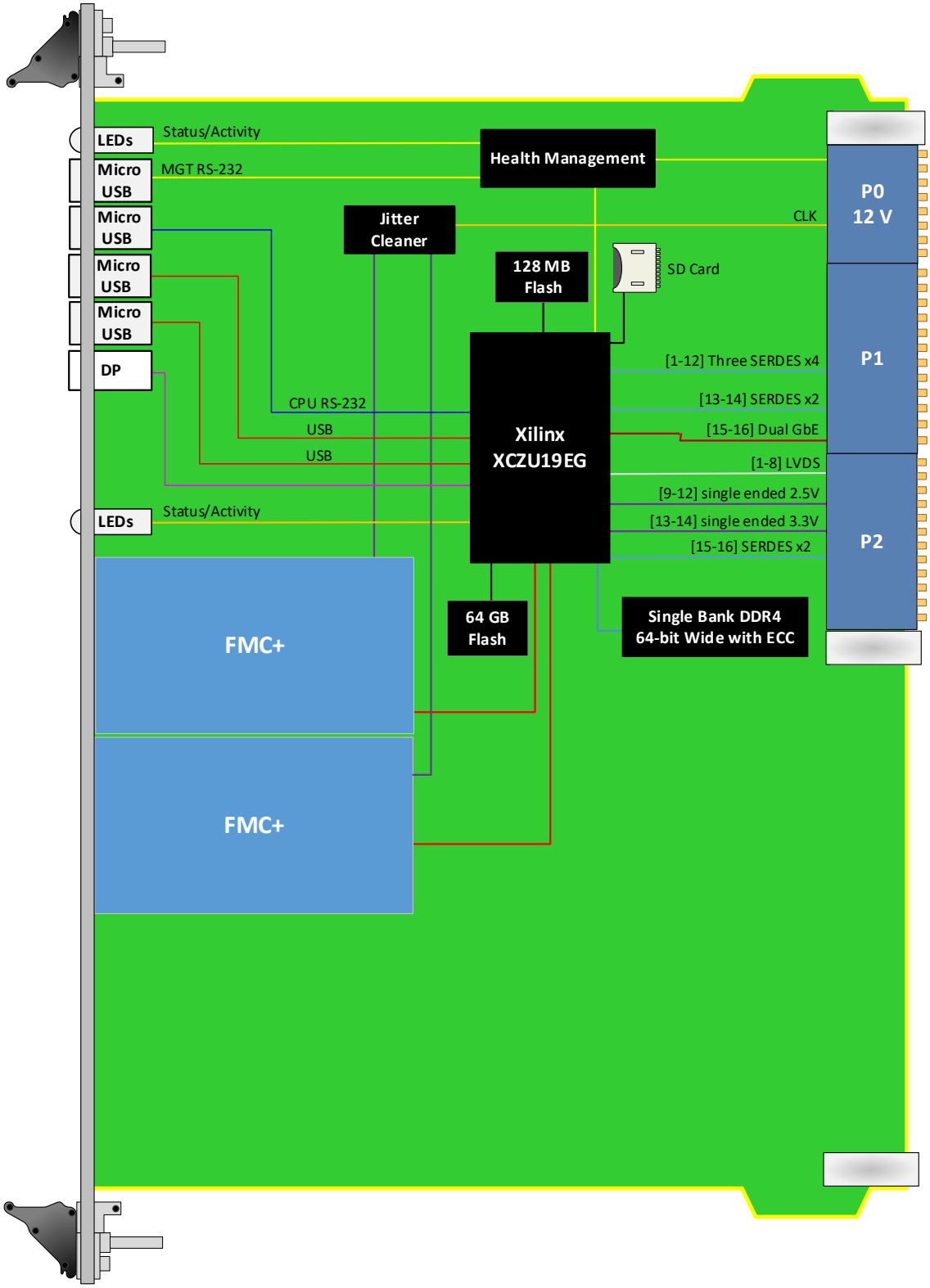
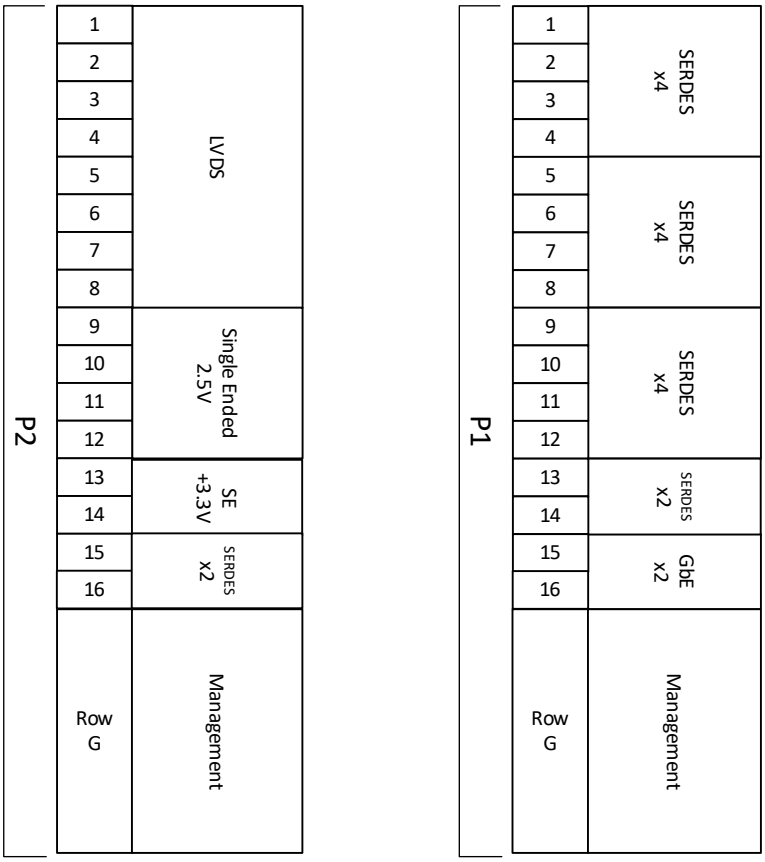


Figure 2: VPX580 Functional Block Diagram

Pinout Block Diagram



Front Panel

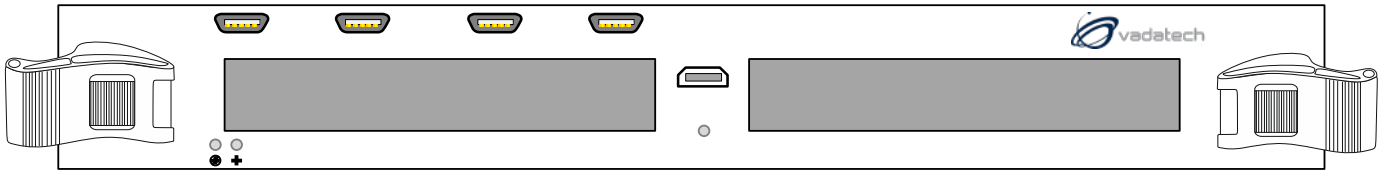


Figure 3: VPX580 Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	6U, 1” pitch
Type	**FPGA**	Xilinx Zynq UltraScale+ with Dual FMC+ sites (w/o eHSPC connector)
Configuration		
Power	**VPX580**	35W FPGA load dependent (without FMC)
Front Panel	**Interface Connectors**	Dual FMC+ Slots
	Micro USB	RS-232 from FPGA and RS-232 from Health Management
		USB 1, USB 2
		Display Port
	LEDs	User defined by the FPGA and Health Management
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	P0: IPMB for Health Management and CLK
		P1: Three x4 fabric, single x2 fabric
		P2: 8 x LVDS, x4 single ended (2.5V), x2 single ended (3.3V) and dual GbE (VITA 46.6)
Software Support	**Operating System**	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX580 – ABC-DEF-GHJ

A = VPX Connector Type	D = FPGA Speed	G = Applicable Slot Profiles
0 = Standard 50u Gold Rugged 1 = KVPX Connectors	1 = Reserved 2 = High 3 = Highest	0 = 5 HP, VITA 48.1
B = Expansion Plane (P2)	**E = Clock Holdover Stability**	**H = Environmental**
0 = P2 Not loaded 1 = P2 Loaded	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification
C = SD Card	**F = PCIe Option (P1) for Data Port 1/2**	**J = Conformal Coating**
0 = No SD Card 1 = SD Card (32 GB)	0 = No PCIe 1 = PCIe/None 2 = None/PCIe 3 = PCIe/PCIe	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX592

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

Contact

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