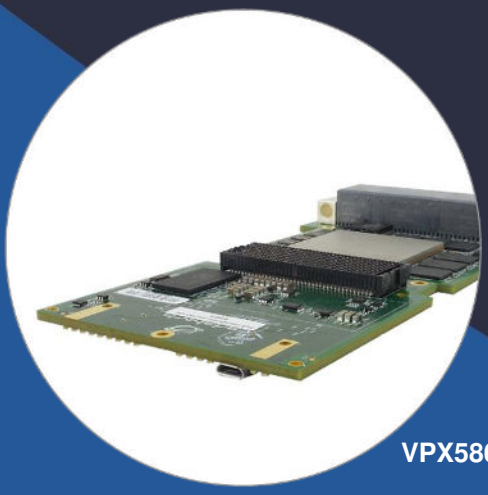
VPX586

Zynq UltraScale+ FPGA, FMC+ Carrier, 3U VPX



VPX586

Key Features

- Xilinx UltraScale+ XCZU19EG FPGA
- Single FMC+ (VITA 57.4) site
- 8 GB of 64-bit wide DDR4 Memory (single bank) with ECC (CPU)
- Dual 4 GB of 32-bit wide DDR4 Memory (FPGA)
- MPSoC with block RAM and UltraRAM
- Health Management through dedicated Processor

Benefits

- FMC+ site on a single module VPX
- Zynq UltraScale+ MPSoC
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX586

The VPX586 is a 3U VPX FPGA Carrier with single FMC+ (VITA 57.4) interface. The unit has an onboard, re-configurable FPGA which interfaces directly to the VPX P1 and P2 connectors and all FMC+ LA/HA/HB pairs (the module does not support HSPCe connector).

The VPX586 is based on Xilinx UltraScale+ XCZU19EG MPSoC FPGA with single FMC+ site. The FPGA has 1968 DSP Slices and 1143k logic cells. The XCZU19EG includes a quad-core ARM application processor, a dual-core ARM real-time processor and a Mali™ graphics processing unit, as well as over 34.6 Mb of block RAM and 36 Mb of UltraRAM.

The FPGA has interface to a single DDR4 memory channel (64-bit wide with ECC) to the ARM CPU, and two 4 GB banks of DDR4 memory channel (32-bit wide) to the Programmable Logic. This allows for large data sizes to be stored during processing and supports ping-pong buffering for data streaming applications.

16 lanes of high-speed SERDES (GTH) are routed to P2 for I/O expansion. These are supported by GPIO (x12 LVDS or x24 single-ended) that could be used for control and monitoring of offboard transceivers connected to the SERDES.

The module has onboard 64 GB of Flash, 128 MB of boot flash.

Figure 1: VPX586

Figure 2: VPX586 w/ heat sink

Block Diagram

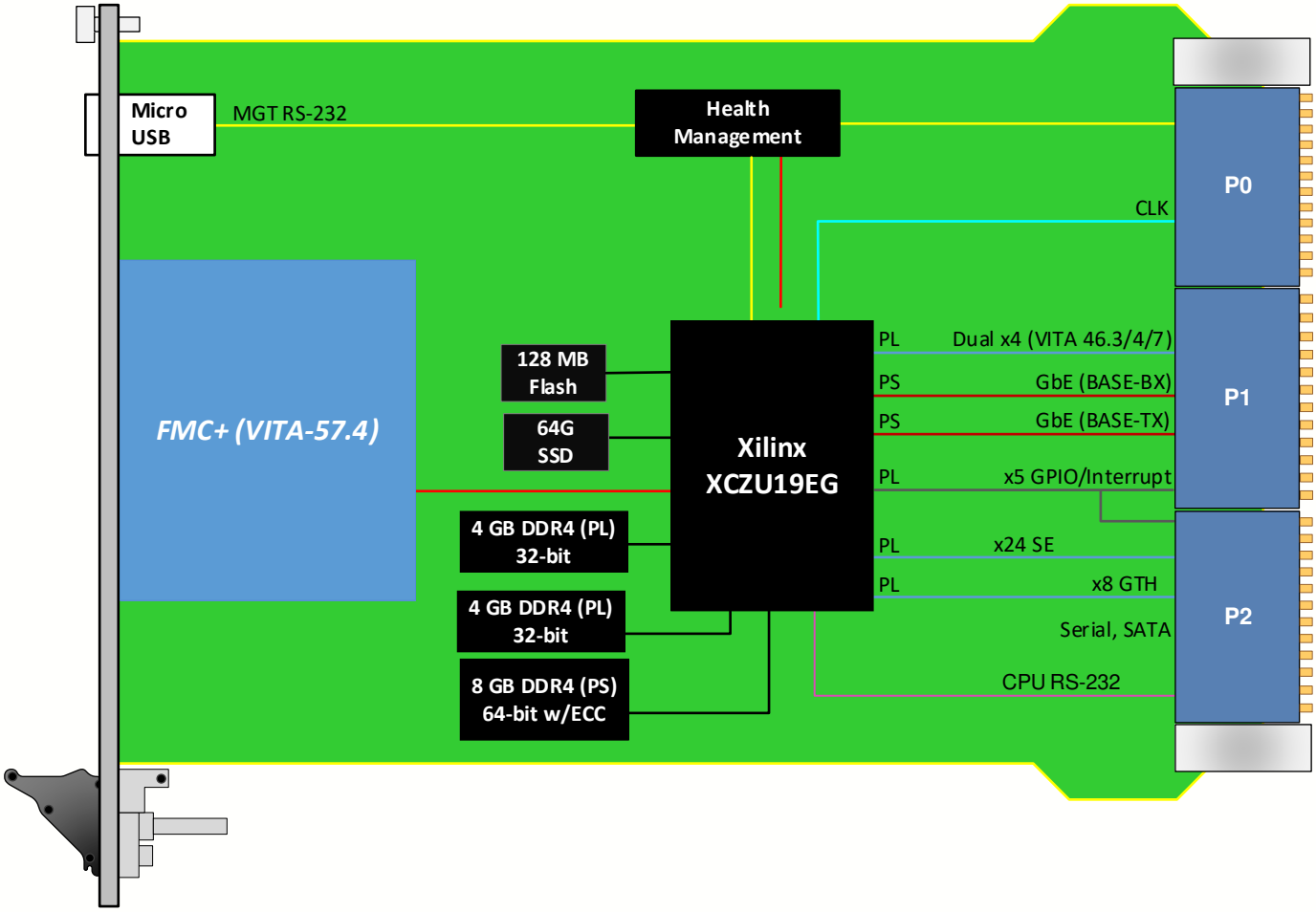

Figure 3: VPX586 Functional Block Diagram

Front Panel

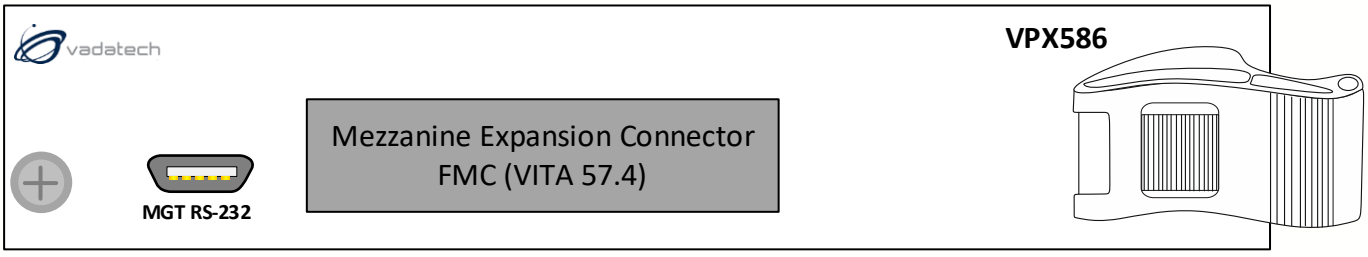

Figure 4: VPX586 Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
Type	**FPGA**	Xilinx Zynq UltraScale+ with FMC+ site
Configuration		
Power	**VPX586**	~30W FPGA load dependent and no FMC+
Front Panel	**Interface Connectors**	Single FMC+ Slot
	Micro USB	RS-232 from Health Management and RS-232 from CPU
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	P0: CLK
		P1: Dual x4 fabric (VITA 46.3, 46.4, 46.7) and Dual GbE (VITA 46.6)
		P2: x12 fabric (configurable) and x12 LVDS
Software Support	**Operating System**	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX586 – A00-D0F-GHJ-K00

A = Front Panel	D = FPGA Speed	G = Applicable Slot Profiles	K = VPX Connector Type
0 = Standard Front Panel 1 = No FMC Slot	1 = Reserved 2 = High 3 = Highest	0 = 5 HP, VITA 48.1	0 = Standard 50u Gold Rugged 1 = KVPX Connectors
		H = Environmental	
		See Environmental Specification	
	F = PCIe Option (P1)*	**J = Conformal Coating**	
	0 = No PCIe 1 = PCIe on lanes 0-3 2 = PCIe on lanes 0-3, 4-7 3 = PCIe on lanes 0-3, 4-7, 8-11	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic	

Notes: *When the ports are not PCIe the lanes are electrically compatible with SRIO, XAUI, and other SERDES protocols.

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX592

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

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