VPX587

300 MHz to 6 GHz Octal Versatile Wideband Transceiver (MIMO), Virtex UltraScale+™, 3U VPX

VPX587

Key Features

- Xilinx Virtex UltraScale+™ XCVU13P FPGA
- Four AD9371s or AD9375s on one module
- Octo complete transceiver signal chain solution
- Tx synthesis bandwidth to 250 MHz
- Rx bandwidth: 8 MHz to 100 MHz
- Health Management through dedicated Processor

Benefits

- High density transceiver with intensive data processing capability
- Observation channels for implementation of error correction functions
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™

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VPX587

The VPX587 is a wideband transceiver in 3U VPX form factor. The unit consists of four AD9371s connected to a Virtex UltraScale+™ XCVU13P FPGA that provide eight transceivers channels. This makes it suitable for signal SDR, BTS, antenna systems, research and instrumentation.

The re-configurable FPGA interfaces directly to wideband transceivers (via JESD204B) and also one bank of DDR4 memory. This allows for maximum buffer sizes to be stored during processing as well as queuing the data to the host connectors.

The module routes x16 SERDES to P1 that can run any protocol (i.e PCIe/SRIO/10G/40G/Aurora) and x8 SERDES with 16 LVDS signals to P2.
The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

Please contact VadaTech for details of Conduction Cooled versions.

Figure 1: VPX587

Figure 2: VPX587 Conduction Cooled

Block Diagram

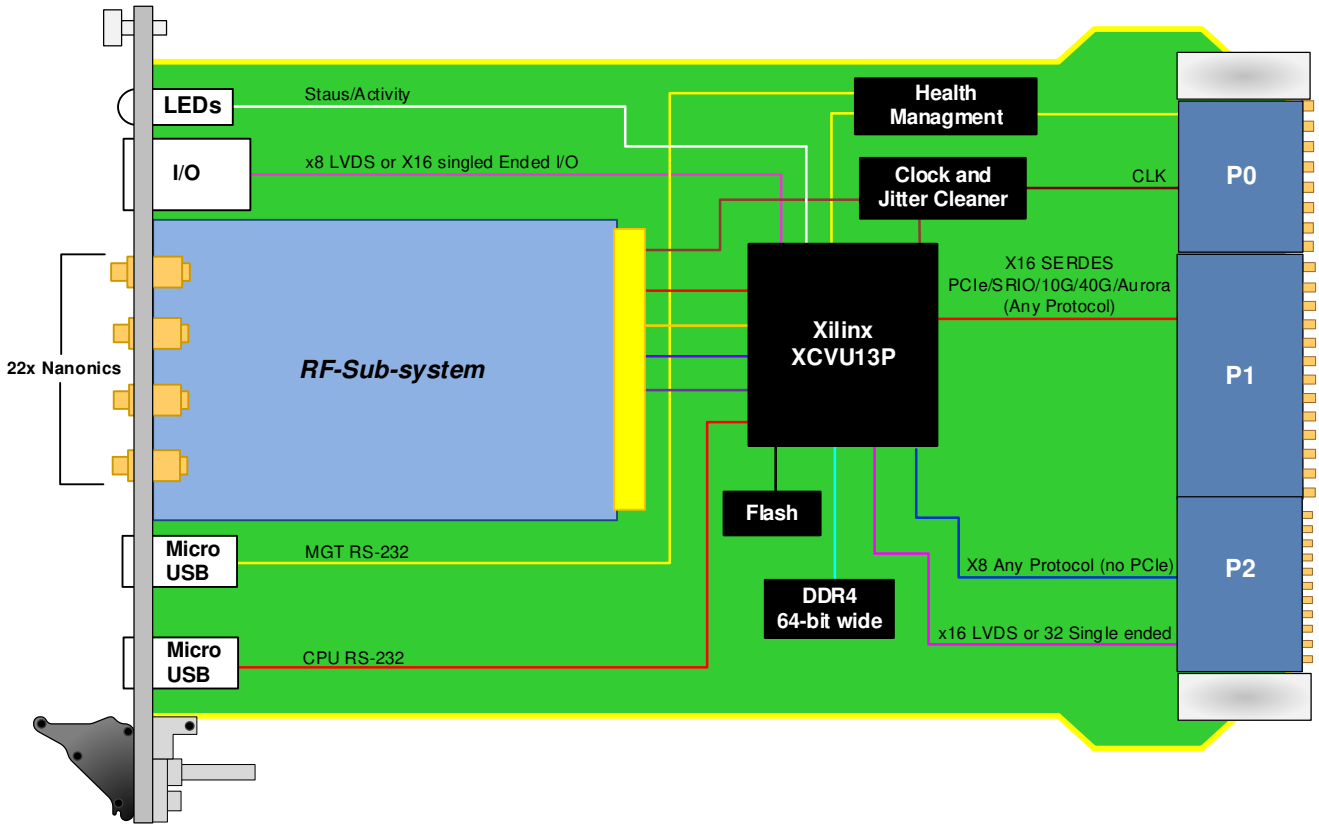

Figure 3: VPX587 Block Diagram

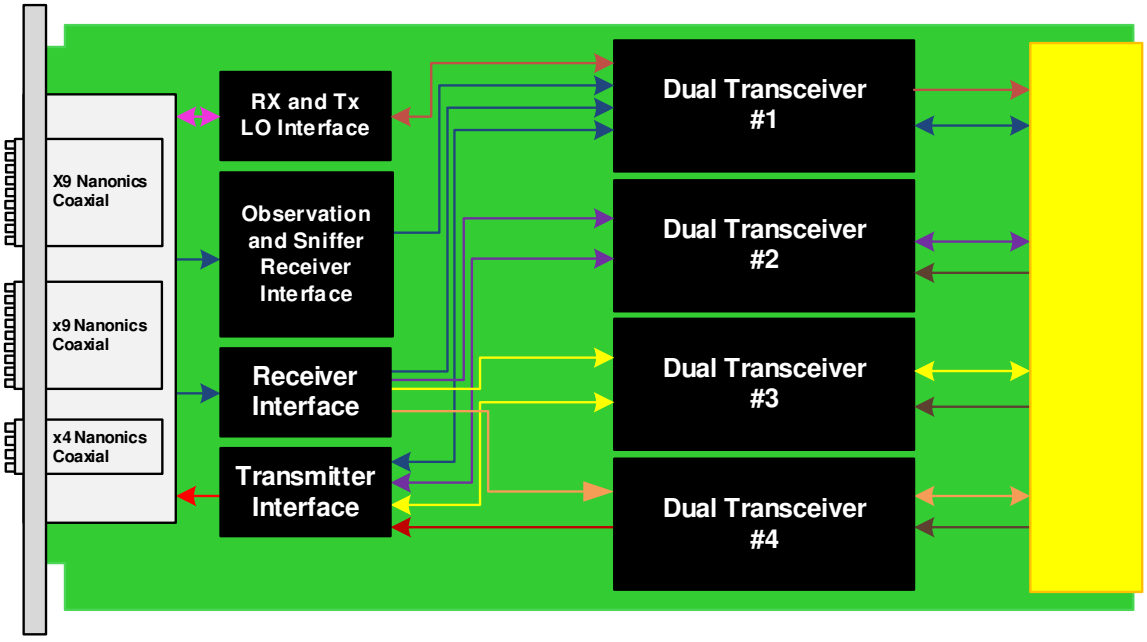

Figure 4: RF Sub-system Block Diagram

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

The VPX587 is compatible with Analog Devices design tools for AD9371.

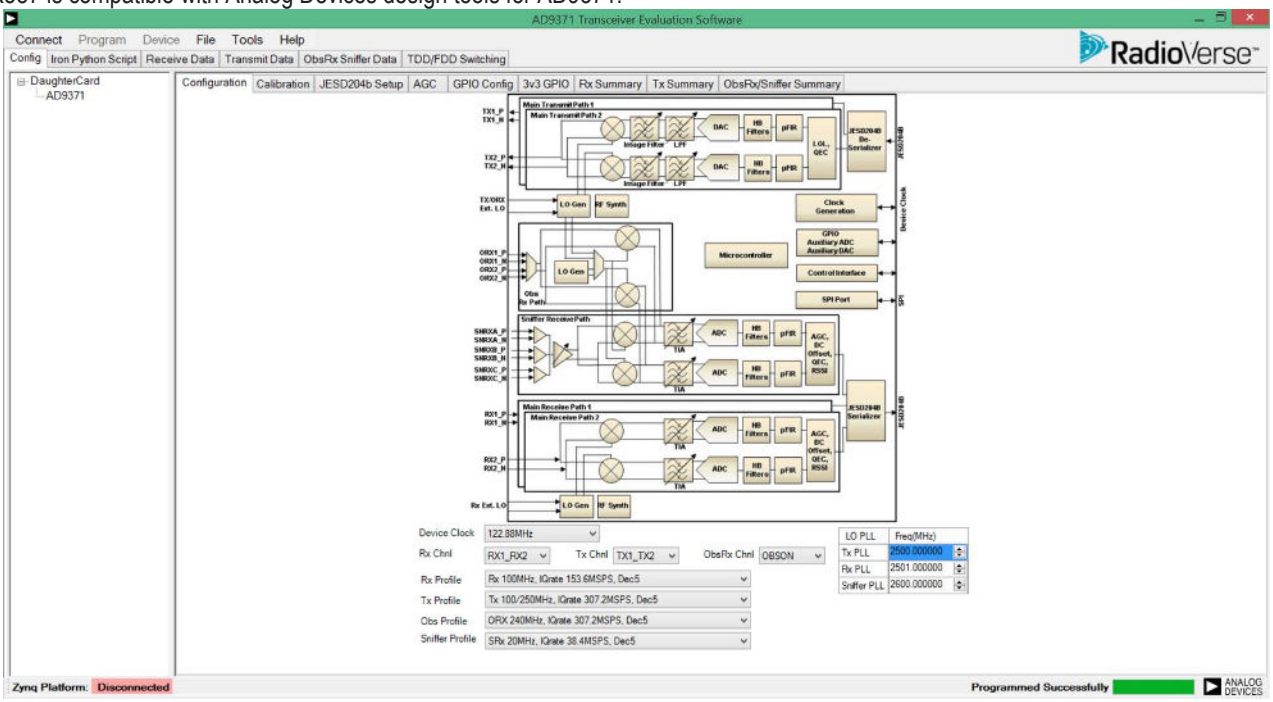

Figure 5: VPX587 Compatible Analog Devices

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
FPGA		Xilinx UltraScale+™ XCVU13P FPGA
Configuration		
Power	**VPX587**	~60W (dependent on FPGA load)
Memory		One bank of DDR4, 64-bit wide (8 GB total)
Front Panel		22 Nanonics Coaxial
	Micro USB	RS-232 from Health Management and RS-232 from FPGA
	LEDs	User defined by the FPGA and Health Management
Onboard Interfaces		JTAG
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	x16 SERDES could be configured as PCIe/SRIO/10GbE/40GbE/Aurora on P1
		x8 SERDES could be configured as SRIO/10GbE/40GbE/Aurora on P2
		x16 LVDS or 32 single-ended on P2
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX587 – ABC-DEF-GHJ

A = RF Direct Clock Sampling	D = FPGA Speed	G = Applicable Slot Profiles
0 = Front Panel 1 = Onboard Wideband PLL	1 = High (-2)* 2 = High (-2LE) 3 = Highest (-3E)*	0 = 5 HP, VITA 46, IEEE 1101 1 = 5HP, VITA 48.1
B = MIMO Device	**E = Clock Holdover Stability**	**H = Environmental**
0 = AD9371 1 = ADD9375	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification
C = VPX Connector Type	**F = PCIe Option (P1)****	**J = Conformal Coating**
0 = Standard 50u Gold Rugged 1 = KVPX Connectors	0 = No PCIe (40GbE, 10GbE, SRIO, etc.) 1 = x4 or x8 PCIe via FPGA 2 = Quad x4, or dual x8 via FPGA	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Notes: *Minimum Order Quantity applies for these FPGA SKU's.

**When the ports are not PCIe the lanes are electrically compatible with SRIO, XAUI, and other SerDes protocols.

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX516

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX592

- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014
Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan
Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR
Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

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