# VRT555A

# Rear Transition Module I/O for VadaTech VPX555



# **Key Features**

- 6U RTM VITA 46
- Very High-Density Connector (VHDCI)
  - o LVDS and M-LVDS
- Loop back on ports RP0/RP1/RP2 and RP3 (ports 14/15 only)
- Interfaces with the VadaTech VPX555

# **Benefits**

- Full System supply from industry leader
- AS9100 and ISO9001 certified company





# VRT555A

The VRT555A is a 6U VPX Rear Transition Module for use with VadaTech VPX555. The module has a VHDCl connector that connects the RP3 MLVDS and LVDS from the VPX555 to the rear. It optionally loops back the RP0/RP1/RP2 ports and RP3 (ports 14/15 only).



Figure 1: VRT555A



Figure 2: VRT555A Front Panel View

# **Block Diagram**

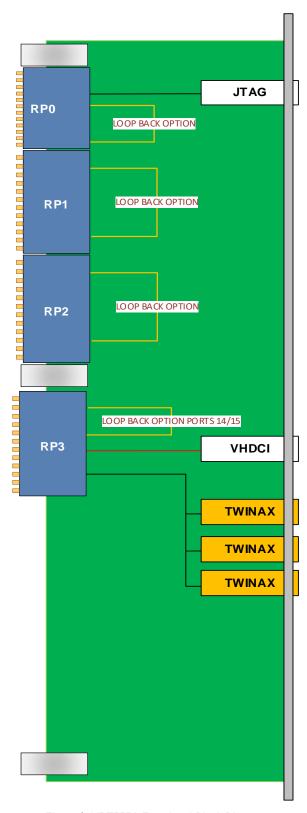


Figure 3: VRT555A Functional Block Diagram

# **Specifications**

Architecture				
Physical	Dimensions	6U, 1" pitch		
FPGA		VPX RTM to interface with the VadaTech VPX555 module		
Configuration				
Power	VRT555A	0.2W		
Memory		None		
Rear Panel		JTAG		
VPX Interfaces	Slot Profiles	See Ordering Options		
Rear IO	RP3	VHDCI		
	Power Supplies	On RP0: 12V		
Other				
MTBF	MIL Hand book 217-F@ TBD hrs			
Certifications	Designed to meet FCC, CE and UL certifications, where applicable			
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards			
Warranty	Two (2) years, see VadaTech Terms and Conditions			

## INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as preconfigured Application-Ready Platforms. Please contact VadaTech Sales for more information.

# **Ordering Options**

## VRT555A - A00-000-GHJ

A = Loop Back		G = Applicable Slot Profiles	
0 = None 1 = Loop Back Enable		0 = 5 HP	
		H = Environmental	
	See Environment		
		J = Conformal Coating	
		0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic	

#### Notes:

## **Environmental Specification**

Air Cooled			Conduction Cooled		
Option H	H = 0	H=1	H = 2	H = 3	H = 4
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

#### Notes:

## **Related Products**



- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner



- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Kintex-7 410T FPGA in FFG-900 package
- High-performance clock jitter cleaner

<sup>\*</sup>Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4)

# **Contact**

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