THE POWER OF VISION

Specifications & Compliance

Many of VadaTech's products comply to VITA® and PICMG® standards. Below is list of several of the related specifications. (VadaTech does not assume responsibility for any inaccuracies below and the specifications are the property of their respective organizations)

Related PICMG Specifications

PIMG No.	Name	Revision ECN	Date	Status	Description
AMC.0	AdvancedMC™ Mezzanine Module	Rev 2.0	11/15/06	Adopted	Defines a mezzanine building block approach for the addition of crucial functionality to a PICMG 3.0 carrier card available from a number of third party suppliers.
		Rev 1.0	1/3/05	Obsolete	Replaced by Rev 2.0
		R1 ECN 001	6/26/06	Obsolete	Incorporated in Rev 2.0
		R1 ECN 002	11/15/06	Obsolete	Incorporated in Rev 2.0
AMC.1	AdvancedMC™ PCI Express and AS	Rev 2.0	10/8/08	Adopted	Defines port usage for PCI Express and Advanced Switching environments on AMC.0
AMC.2	AdvancedMC™ Ethernet	Rev 1.0	3/1/07	Adopted	Defines port usage for Ethernet on AMC.0
AMC.3	AdvancedMC™ Storage	Rev 1.0	8/25/05	Adopted	Defines port usage for Fibre Channel on AMC.0
AMC.4	AdvancedMC™ Serial RapidIO	Rev 1.0	7/11/09	Adopted	Defines port usage for Se

PIMG No.	Name	Revision ECN	Date	Status	Description
MTCA.0	MicroTCA®	Rev 1.0	7/6/06	Adopted	Defines a system architecture that uses AdvancedMC mezzanine cards plugged directly into a backplane without modifications.
MTCA.1	Air Cooled Rugged MicroTCA®	Rev 1.0	3/19/09	Adopted	Defines Ruggedized version of MicroTCA for exterior and mobile communications applications.
MTCA.2	Hardened Air Cooled MicroTCA®	Errata	5/20/13	Adopted	MicroTCA.2 R1.0 Errata
		Rev 1.0	5/1/13	Adopted	Expands the market for MicroTCA into commercial and military ruggedized applications
MTCA.3	Hardened Conduction Cooled MicroTCA®	Rev 1.0	2/24/11	Adopted	Expands the market for MicroTCA into commercial and military ruggedized applications
MTCA.4	MicroTCA® Enhancements for Rear I/O and Precision Timing	Errata	8/1/12	Adopted	MicroTCA.4 R1.0 Errata
		Rev 1.0	8/22/11	Adopted	Defines an AMC and a corresponding MicroRTM module set for rear I/O along with an appropriate MicroTCA shelf.
3.0	AdvancedTCA® (Base Specification)	Rev 3.0	3/24/08	Adopted	Incorporates ECN's to R2.0 and additional CR's
		Rev 2.0	3/18/05	Obsolete	Replaced by Rev 3.0
		R2 ECN001	6/15/05	Obsolete	Adds ShMC Cross Connect. Replaced by Rev 3.0
		R2 ECN002	4/29/06	Obsolete	Replaced by Rev 3.0

PIMG No.	Name	Revision ECN	Date	Status	Description
3.0	AdvancedTCA® (Base Specification)	Rev 1.0	12/30/02	Obsolete	The PICMG 3.0 “core” specification specifies board, backplane and shelf mechanicals; power distribution and the connectivity required for system management. Replaced by Rev 2.0.
		R1 ECN 001	1/21/04	Obsolete	Changes incorporated in Rev 2.0
3.1	AdvancedTCA® Ethernet	Rev 2.0	8/3/12	Adopted	Develops enumerated requirements that incorporate 1000BASE-KX, 10GBASE-KX4 and 10GBASE-KR fabric options into Revision 2.0 of the PICMG 3.1 specification.
		Rev 1.0	1/22/03	Obsolete	Defines how Ethernet and Fibre Channel are mapped onto PICMG 3.0.
3.2	AdvancedTCA® InfiniBand	Rev 1.0	1/22/03	Adopted	Defines how InfiniBand transport is mapped onto PICMG 3.0
2.0	CompactPCI®	Rev 1.0	1/22/03	Adopted	Defines how InfiniBand transport is mapped onto PICMG 3.0
		R3 ECN 002	1/23/02	Adopted	Adds Geographical to Logical Address Mapping to Rev 3.0 Download ECN 002
		R3 ECN 001	10/1/08	Abandoned	PCI-X on CompactPCI
		R2.1	9/2/97	Obsolete	Defines a IEEE 1101.1 (Eurocard) PCI form factor, and assign a PCI pinout on the IEC 1076-4-101 family of 2 millimeter hard metric connectors. Replaced with Rev 3.0

PIMG No.	Name	Revision ECN	Date	Status	Description
2.1	Hot Swap	Rev 2.0	1/17/01	Adopted	Incorporates ECRs for: Enhanced software connection architecture, 3.3 volt 66 MHz support, PCI-X compatibility, Compliance language
		Rev 1.0	8/3/98	Obsolete	Incorporates Hot Swap pin sequencing and other enhancements. Replaced by Rev 2.0
2.3	PMC I/O	Rev 1.0	9/9/98	Adopted	Defines user IO pin mappings from IEEE 1386 PMC sites to J3/P3, J4/P4, and J5/P5 on a CompactPCI backplane.
2.5	Telephony	Rev 1.0	4/3/98	Adopted	Defines the utilization of pins for the computer telephony functions of TDM bus, telephony rear IO, 48 VDC and ringing distribution.
2.9	Management	Rev 1.0	2/2/00	Adopted	Defines a secondary system management bus for CompactPCI.
		R1 ECN	5/20/02	Adopted	Defines CompactPCI slot connectivity data
2.10	Keying	Rev 1.0	10/1/99	Adopted	Defines use of the keying mechanisms defined in IEC 1076-4-101 for the J4/P4 connector and in IEEE 1101.10 for handle and cardguide hardware.
2.11	Power Interface	Rev 1.0	10/1/99	Adopted	Defines use of the keying mechanisms defined in IEC 1076-4-101 for the J4/P4 connector and in IEEE 1101.10 for handle and cardguide hardware.

Related VITA Specifications

Specification	Name	Description	Status
ANSI/VITA 1.1-1997 (S2011)	VME64x Extensions	This specification is an extension of the ANSI/VITA 1-1994, VME64 specification. It defines a set of features that can be added to VME32 and VME64 boards, backplanes and subracks. These features include a 160 pin connector, a P0 connector, geographical addressing, voltages pins for 3.3V, a test and maintenance bus, and EMI, ESD, and front panel keying per IEEE 1101.10.	ANSI Stabilized
ANSI/VITA 1.5-2003 (R2009)	VME 2eSST	This specification is an extension of the ANSI/VITA 1-1994, VME64 and ANSI/ VITA1.1-1997, VME64x specifications. It defines a transfer protocol, based upon source synchronous concepts, that permits the VMEbus to operate at rates to at least 320MB/s. As technology improves, this rate can be extended to higher levels. The 2eSST protocol requires low skew between signals and monotonic rising and falling edges on the signals. To meet these requirements, limited length backplanes, special backplane topologies and/or enhanced transceivers are required. The specification calls for enhanced bus transceivers with controlled rise and fall times, tightly defined thresholds, low part to part skew and LVTTL levels. During the development of this standard, specific transceivers were developed to meet these requirements.	ANSI Ratified
ANSI/VITA 1.5-2003 (R2009)	VME 2eSST	The VME Switched Serial (VXS) specification comprises this base standard defining physical features of VXS components, coupled with a set of protocol layer standards to define the specific serial interconnect used in a system implementation.	ANSI Ratified

Specification	Name	Description	Status
		The VXS base specification defines physical features that enable high-speed communication in a VME compatible system. These features include: addition of a high speed connector to the VME64x board in the P0/J0 position, a 6U by 160mm by 6HP Eurocard format board with many high speed connectors which may act as a switch, and the backplane/ chassis infrastructure needed to support these features. In addition to defining a high -speed connector in the P0/J0 area, VXS also defines alignment and keying features which may be used to protect this and future alternate connectors. The ratio of one high-speed connector per payload board to many on the switch card lends itself to a star topology where each payload card is connected to a central switch. For higher reliability and/ or load balancing, two switch cards may be used in a dual star configuration. Interswitch links may be included for reliability and load balancing reasons as well. Although this topology is not required it is a natural fit for the system features.	
ANSI/VITA 46.0-2007 (R2013)	VPX: Base Specification	Commonly known as VPX, this specification family defines entirely new high-speed connectors in part to carry mappings for popular switched serial fabrics including Gigabit Ethernet, PCI Express, Serial RapidIO, InfiniBand, and Aurora. It also defines a new increased power envelope including a 48V profile, and additional cooling methods. The base standard does not address the possible serial fabric configurations available in systems which utilize the standard	ANSI Ratified

Specification	Name	Description	Status
ANSI/VITA 65.0-2010 (R2012)	OpenVPX Architectural Framework for VPX	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications protocols, utility, and power definitions provided by specific VPX standards and then describes a series of standard profiles that define slots, backplanes, modules, and standard development chassis.	ANSI Ratified
ANSI/VITA 57.1-2008	FMC: FPGA Mezzanine Cards Base Specification	This specification describes an IO mezzanine module, which shall connect to, but is not limited to, 3U and 6U form factor cards. This mezzanine module is in a smaller form factor, when compared to PMC/XMC modules and assumes that it will be connected to a FPGA device or other device with reconfigurable IO capability. This standard describes FMC IO modules and introduces an electro-mechanical standard that creates a low overhead bridge. This is between the front panel IO, on the mezzanine module, and an FPGA processing device on the carrier card, which accepts the mezzanine module.	ANSI Ratified
ANSI/VITA 42.0-2008	XMC: Switched Mezzanine Card Base Specification	Specific goals include supporting: - A high-speed switched interconnect. - Open, standardized technologies for switched fabrics. - Standard PMC form factors. - Compatibility with existing PMC specifications. - PMC, XMC, or dual-mode mezzanine cards. - PMC, XMC, or dual-mode carriers. - Standard VME, CompactPCI, Advanced TCA, and PCI Express carriers. - Standard PMC stacking heights. - Optional conduction cooling.	ANSI Ratified

Specification	Name	Description	Status
		In support of these goals, this document specifies the mechanical and generic electrical requirements necessary to serve as a basis for any number of protocol layer standards built on and complying with this standard.	
ANSI/VITA 32-2003 (R2009)	Processor PMC	The complete physical (mechanical) and the environmental layers are retained as specified in the IEEE 1386 CMC (“Common Mezzanine Card”) standard except as noted in this document. If the information in this document contradicts IEEE 1386 or IEEE 1386.1, this document takes precedence. Processor PMC cards are used where modular attachment of a processor is desired. These processor PMC cards may be used in conjunction with PMC I/O cards, traditional PCI cards, or with directly attached PCI components. As such, Processor PMCs increase the modularity of a computer system and thus complement, rather than compete with, the existing family of PMC cards. Processor PMC cards are expected to electrically operate with existing carrier boards (or motherboards); that is, while the carrier may be redesigned to take advantage of the enhanced functions that are offered by this standard, such a redesign should not be a requirement to insure proper operation. Indeed, Processor PMCs shall be specifically enabled to operate as master/host CPUs; otherwise, such cards revert to traditional PMC modes, operating as intelligent slave/target processor boards.when that support is required within PMC and Processor PMC designs.	ANSI Ratified