AMC502

FPGA Carrier with Dual FMC, Kintex-7, AMC

AMC502

Key Features

- AMC FPGA carrier for dual FPGA Mezzanine Card (FMC) per VITA 57
- Double module, mid-size (full-size optional)
- Xilinx Kintex-7 FPGA (XC7K420T) in a FFG1156 package
- AMC Ports 4-7 and 8-11 are routed to FPGA per AMC.1, AMC.2 and AMC.4 (protocols such as PCIe, SRIO, XAUI, etc. are FPGA programmable)
- 32 MB of Flash memory

Benefits

- The LVDS cross-bar switch provides improved clock flexibility
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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AMC502

The AMC502 is an AMC FPGA Carrier with dual FMC (VITA 57) interface. This allows the versatility of various FMC modules to be implemented. The module is compliant to the AMC.1, AMC.2 and/or AMC.4 specifications.

The onboard, re-configurable FPGA interfaces directly to AMC FCLKA, TCLKA-D, FMC DP0-3, and all FMC LA/HA/HB pairs. Port 3 can be routed as LVDS.

AMC502 has an onboard crystal-referenced clock source to provide at least 125 MHz as GTX reference inputs for PCIe, SRIO and GbE. The iMX6 CPU is a quad core ARM processor at 1 GHz for power-efficient distributed processing.

Figure 1: AMC502

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

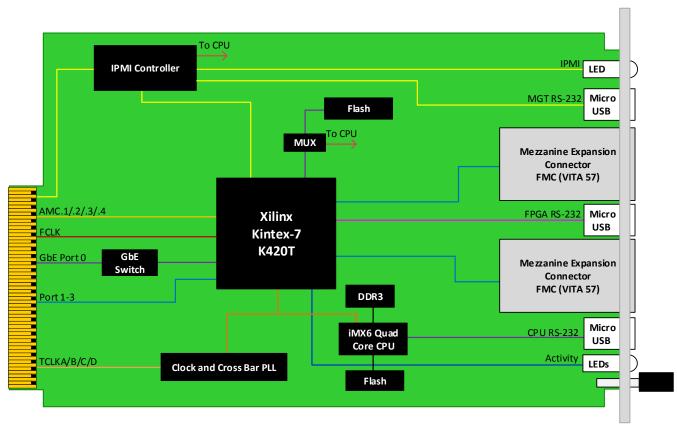[Xilinx Vivado Design Suite](#), [Xilinx System Generator for DSP](#).

Block Diagram

Figure 2: AMC502 Functional Block Diagram

AMC502 – FPGA Carrier with Dual FMC, Kintex-7, AMC

Specifications

Architecture		
Physical	**Dimensions**	Double module, mid-size (full-size optional)
		Width 5.85" (148.5 mm)
		Depth 7.11" (180.6 mm)
Type	**AMC FPGA Carrier**	Xilinx Kintex-7 Device (XC7K420T)
		Dual FMC slots
		iMX6 Quad CPU
Standards		
AMC	**Type**	AMC.1, AMC.2, AMC. 3 and AMC.4 (FPGA programmable)
Module Management	**IPMI**	IPMI v2.0
PCIe	**Lanes**	Dual x4 or x8 PCIe Gen 2 via FPGA to AMC
SRIO	**Lanes**	Dual x4 via FPGA to AMC
Ethernet	**GbE**	Ports 0 and 1
Configuration		
Power	**AMC502**	~20W, application specific
Environmental	**Temperature**	See Ordering Options and Environmental Spec Sheet
		Storage Temperature: –40° to +85°C
	Vibration	Operating 9.8 m/s^2 (1G), 5 to 500 Hz
	Shock	30G on each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	**Interface Connectors**	Single FMC Slot
		Front panel dual FMC, IPMI RS-232, FPGA RS-232, CPU RS-232
	LEDs	IPMI management control
		Debug (user defined) LED
	Mechanical	Hot-swap ejector handle
Software Support	**Operating System**	Linux, VxWorks and Windows
Other		
MTBF		MIL Hand book 217-F@ TBD hrs
Certifications		Designed to meet FCC, CE and UL certifications, where applicable
Standards		VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards
Warranty		Two (2) years, see VadaTech Terms and Conditions

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

AMC502 – A0C-DEF-G0J

A = I/O Clock Signal Routing	D = FPGA	G = Clock Holdover Stability
0 = Standard routing 1 = CMS routing	0 = Reserved 1 = Reserved 2 = XC7K420T	0 = Standard (XO) 1 = Stratum-3 (TCXO)
	E = FPGA Speed	
	1 = Low* 2 = High 3 = Highest*	
C = Front Panel	**F = PCIe Fabric**	**J = Temperature Range and Coating**
1 = Reserved 2 = Mid-size 3 = Full-size 4 = Reserved 5 = Mid-size, MTCA.1 (captive screw) 6 = Full-size, MTCA.1 (captive screw)	0 = No PCIe 1 = PCIe on Ports 4-7 2 = PCIe on Ports 8-11 3 = PCIe on Ports 4-11	0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane** 7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic**

Notes: *Minimum purchased required contact sales for details.

**Conduction cooled; temperature is at edge of module. Consult factory for availability

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Related Products

FMC210

- FPGA Mezzanine Card (FMC) per VITA 57
- Single ADC 10-bit @ 2.6 GSPS (EV10AS150B)
- 5 GHz Full Power Input Bandwidth (–3dB)

FMC214

- Dual complete transceiver signal chain solution using Analog Devices AD9361 transceiver
- Frequency range 70 MHz to 6 GHz with instantaneous bandwidth from 200 kHz to 56 MHz
- MIMO transceiver is Time Domain Duplex (TDD) and Frequency Domain Duplex (FDD) compatible

FMC223

- FPGA Mezzanine Card (FMC) per VITA 57
- Single module DAC 14-bit @ 2.5 GSPS (AD9739)
- 2 Vpp differential Analog output swing

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014

Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan

Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR

Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

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