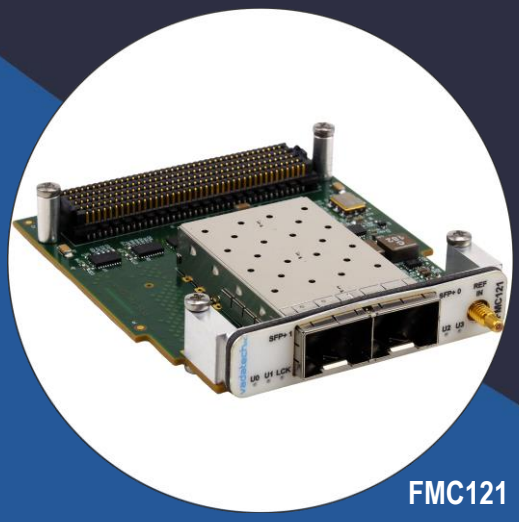
FMC121

Dual zSFP+/SFP28 (protocol agnostic)



FMC121

Key Features

- FPGA Mezzanine Card (FMC) compatible with VITA 57.1
- Two zSFP+/SFP28 cages (max speed 10G)
    - For higher speed consider FMC118
- Onboard Fractional PLL to generate any clock
- Front panel clock allows synchronization of the PLL to an external clock source
- Protocol agnostic (i.e. 1GbE, 5GbE, 10Gb, Aurora, etc.)
- Compact assembly

Benefits

- Single module provides Dual 10Gb, 28G
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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FMC121

The FMC121 is a FPGA Mezzanine Card (FMC) compatible with VITA 57.1 FMC carriers. It has two zSFP+/SFP28 cages which allows for Dual optics to be routed to DP0+/- and DP4+/- pins. The module max speed is 10G for higher speed consider FMC118.

The FMC121 is protocol-agnostic and has a low jitter fractional PLL which can lock to CLK2 and CLK3 coming from the Carrier or be free running. The fractional PLL can generate two separate clocks to the two GBT clock pins and can provide two more additional clocks on CLK0 and CLK1 for the carrier. Further the PLL could also synchronize to an external clock source via its front panel SSMC.

Figure 1: FMC121

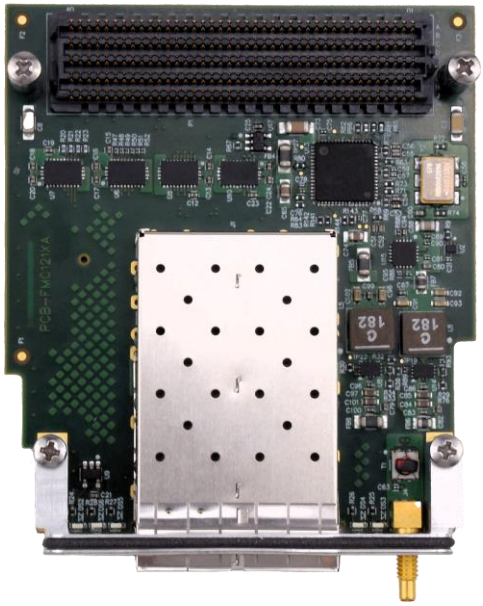


Figure 2: FMC121 Top View

Block Diagram

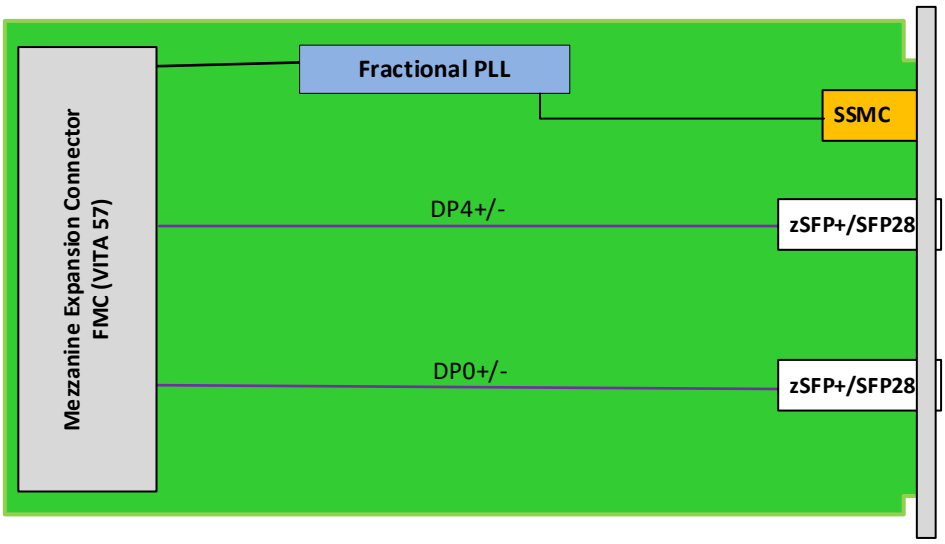


Figure 3: FMC121 Functional Block Diagram

Front Panel

Figure 4: FMC121 Front Panel View

Specifications

Architecture		
Physical	**Dimensions**	Single Module
		Width: 2.71” (69 mm)
		Depth: 3.01” (76.5 mm)
Type	**FMC**	Dual zSFP+/SFP28
Standards		
FMC	**Type**	ANSI/VITA 57.1 – 2008 (exceeds standard height)
Configuration		
Power	**FMC121**	Transceiver dependent
Environmental	**Temperature**	See Ordering Options
		Storage Temperature: –40° to +85°C
	Altitude	40,000 ft non-operating
	Vibration	Operating 9.8 m/s2 (1G), 5-500 Hz
	Shock	Operating 30Gs each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	**Interface Connectors**	Dual zSFP+/SFP28
	LEDs	Status (on back of the board)
Software Support	**Operating System**	Agnostic
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

FMC121 – AB0-000-G0J

A = Number of 10GBASE-SR Transceivers *		G = FMC Board Spacing
0 = None X = Number of Transceivers		0 = 10 mm (per VITA 57 specification) 1 = Reserved 2 = Reserved
B = Number of 10GBASE-LR Transceivers *		
0 = None X = Number of Transceivers		
		J = Temperature Range and Coating
		0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane** 7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic**

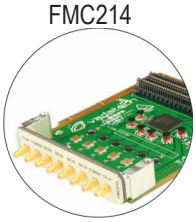
Notes: * Enter number of transceivers required. Total A+B cannot exceed two. Please contact VadaTech sales for other transceiver options.
** Conduction cooled; temperature is at edge of module. Consult factory for availability.

Related Products

VPX592

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- 20 GB of DDR4 Memory (2 banks of 64-bit wide, and single bank of 32-bit wide)

FMC214



- Dual complete transceiver signal chain solution using Analog Devices AD9361 transceiver
- Frequency range 70 MHz to 6 GHz with instantaneous bandwidth from 200 kHz to 56 MHz
- MIMO transceiver is Time Domain Duplex (TDD) and Frequency Domain Duplex (FDD) compatible

AMC585

- Xilinx UltraScale+ XCZU19EG FPGA
- Single FMC+ (VITA 57.4) site
- MPSoC with block RAM and UltraRAM

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014
Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan
Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR
Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

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