PCI599

PCIe FPGA with Quad QSFP-DD
XCVP1802 Versal™ Premium Series

PCI599

Key Features

- PCIe x16 or any protocol on the x16 SERDES
- AMD Versal™ Premium Series XCVP1802 FPGA
- Quad QSFP-DD (Double Data Rate) ports
- SyncE Master/Slave
- PLL to lock to an external 1PPS or an external sinewave clock up to 400Mhz
- Dual x8 SERDES lanes plus additional 24 LVDS pairs for direct connection to neighboring FPGA card(s)
- Single bank of 64-bit wide DDR-4 Memory for a total of 8 GB with ECC
- Dual bank of 64-bit wide DDR-4 Memory 32GB per bank with ECC (64 GB total) as DIMMs
- Active cooling or passive cooling (utilizing chassis cooling such as VadaTech VT808 chassis)

Benefits

- Based on the widely-used VadaTech PCI596/PCI597
- Strong BSP support and example code to support system bring-up
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

PCI EXPRESS

vadatech
THE POWER OF VISION

PCI599

The PCI599 is based on the AMD XCVP1802 Versal™ Premium Series FPGA, which provides over 14,000 DSP slices with total memory of PL 994Mb and 3,360,896 LUTs. The FPGA interfaces to the quad QSFP-DD (Double Data Rate) modules. The Module has a single DDR4 memory bank that is 64-bit wide with ECC for a total of 8GB and an additional two DIMM each 64-bit wide with ECC for total of 64GB. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

PCI599 has a PLL that can lock into an external clock such as 1PPS and/or to a sinewave clock up to 400MHz. The PCI599 could run as SyncE Master and/or Slave. The module provides clocks output which could be connected to adjacent PCI599 modules to allow synchronized between modules.

PCI599 has x16 PCIe edge connector routed to the FPGA PCIe hard IP block. The x16 SERDES going to the edge connector could be configured to run any protocol and integrated, for example, into VadaTech's VT808 chassis. The x16 lanes could be bifurcated to dual x8 or quad x4 lanes (due to limited PCIe hard IP in this chip, separate soft IP cores purchased from AMD/Xilinx would be required for bifurcation). In addition, there are 16 uncommitted SERDES routed to a dual x8 expansion connector, providing direct connectivity to a neighboring FPGA (e.g. via Aurora, 10/40GbE, SRIO, PCIe) without the need to go through the host. Further the module has x24 LVDS pairs to a connector which could be configured as two single ended signals per pair.

Figure 1: PCI599

The Quad QSFP-DD cages could take 400/200/100Gb as well as 40Gb optical transceiver. Each optical modules could be bifurcated to Quad 1/10/25/58/112Gb lanes for a total of 32 ports (at 112Gb only 16 lanes are available). The optical modules are protocol-agnostic and could take a mix of transceiver. The QSFP-DD modules are routed to the GTM transceivers on the FPGA which can operate at 1/20/25/58G/112G per lane. A GbE RJ45 port is also provided.

Options for active cooling of the module or passive cooling. The passive cooling requires a chassis that forces air over the PCI599 heat sink, such as VadaTech's VT808 chassis.

Reference Design

VadaTech provides a reference design implementation for our FPGAs, complete with VHDL source code and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is intended to prove out the hardware for engineering/factory diagnostics and customer acceptance of the hardware, and can be used as a starting point for developing an end application.

Block Diagram

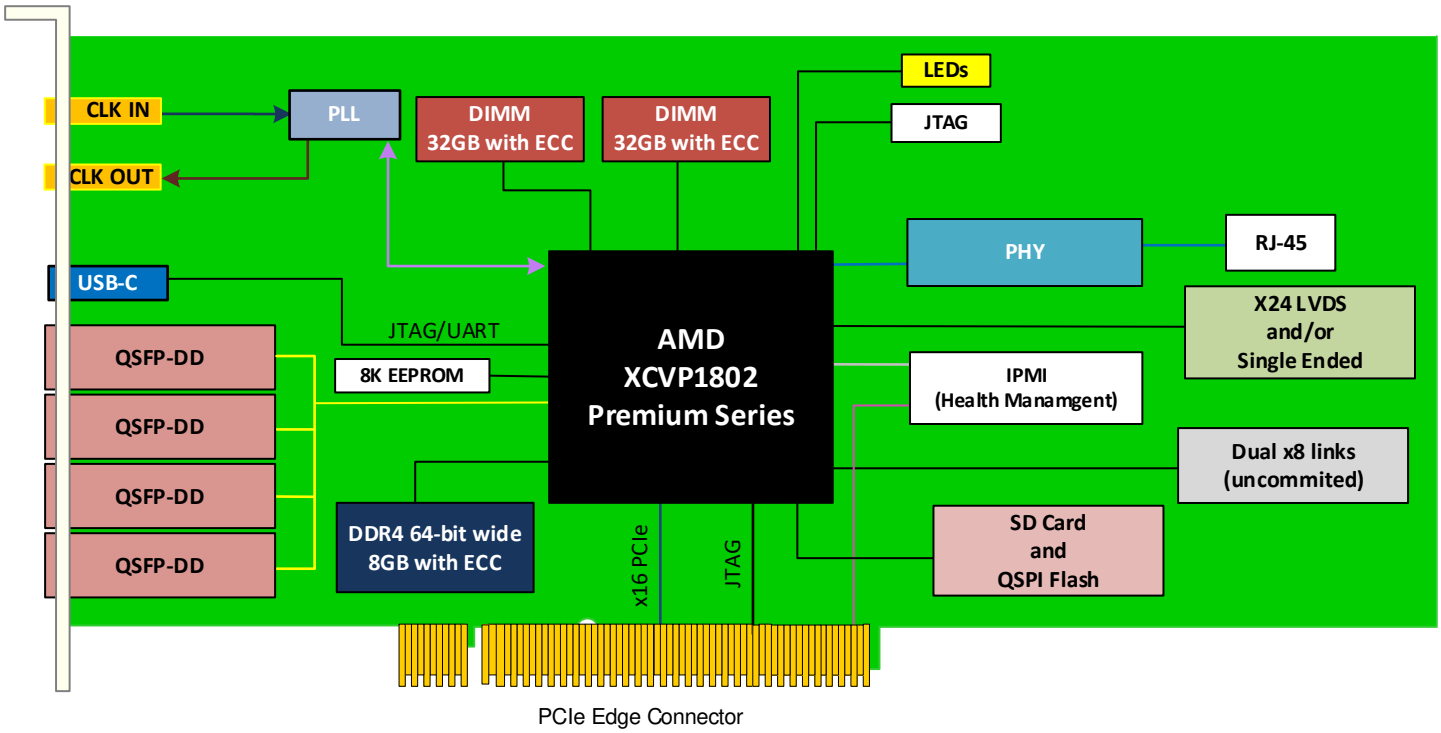

Figure 4: PCI599 Functional Block Diagram

Specifications

Architecture		
Physical	**Dimensions**	Double Module
		Width: 4.37” (111 mm)
		Depth: 12.3” (312 mm)
Type	**PCIe Network**	PCIe FPGA with Quad QSFP-DD
Standards		
PCIe	**Lanes**	X16 or any protocol
Configuration		
Power	**PCI599**	100W (FPGA load dependent and number of optical modules)
Environmental	**Temperature**	See Ordering Options
		Storage Temperature: –40° to +85°C
	Vibration	Operating 9.8 m/s^2 (1G), 5 to 500 Hz
	Shock	30Gs on each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	**Interface Connectors**	SSMC for External clock input/output
		Quad QSFP-DD
		FPGA RS-232 and IPMI Health management as well as HSDP thru USB Type C
		RJ-45, Dual x8 SERDES, 24 LVDS via ARC6 connector style
	LEDs	Status LED
Software Support	**Operating System**	N/A
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

PCI599 – A00-DE0-0HJ

A = Optical modules*	D = Cooling Method	
0 = None 1 = 200G SR4 (50G-PAM4) 2 = 400G SR8 (50G-PAM4) 3 = 100G MTP/MPO SR 4 = 100G MTP/MPO LR (1km) 5 = 100G MTP/MPO LR (10km) 6 = 40G MTP/MPO (SR) 7 = 40G WDM (SR)	0 = Passive cooling (chassis provides cooling) 1 = Active cooling	
	E = FPGA Speed	**H = Temperature Range**
	1 = Slowest (-1)** 2 = Mid (-2) 3 = Highest (-3)**	0 = Commercial (–5° to +50°C) 1 = Industrial (–20° to +65°C)
		J = Conformal Coating
		0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic 3 = Parylene

Notes: *Qty four is shipped with the module, if a mix of modules are needed, please contact VadaTech Sales Team member

**Minimum order quantity applies for these FPGA SKU's and/or memory option

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Related Products

VT808

- 3U Chassis that accepts four standard x16 PCIe Gen5 style modules
- The chassis is designed specially for the FPGA modules that allows SERDES to be re-configured to any protocol
- 400W per module

PCI598

- PCIe x16 or any protocol on the x16 card edge SERDES
- PCIe bifurcation to 2x8 or 4x4
- AMD Versal™ Premium Series XCVP1902 FPGA

PCI590

- PCIe x16 or any protocol on the x16 SERDES
- 72 fiber transceivers egress ports at 10G and/or 25G per lane
- AMD Versal™ Premium Series XCVP1802 FPGA

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014
Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan
Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR
Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

Choose VadaTech

We are technology leaders

- First-to-market silicon
- Constant innovation
- Open systems expertise

We commit to our customers

- Partnerships power innovation
- Collaborative approach
- Mutual success

We deliver complexity

- Complete signal chain
- System management
- Configurable solutions

We manufacture in-house

- Agile production
- Accelerated deployment
- AS9100 accredited

vadatech
THE POWER OF VISION

DOC NO. 4FM737-12 REV 01 | VERSION 1.5 – JUN/2520