UTC006

3rd Gen MicroTCA Carrier Hub (MCH) 40/10GbE/PCIe/ FPGA/SRIO, Double Module

UTC006 (PCIe)

UTC006 (FPGA)

Key Features

- Fabric options include PCIe Gen3, 40/10GbE, SRIO, Cross Bar Switch (CBS) or Xilinx Virtex-7 690T FPGA for complete flexibility
- Front panel fabric expansion, e.g. quad Ports for PCIe Gen 3 (x4, x8, or x16)
- PLL synthesizer for generating any clock frequency disciplined to GPS/SyncE/IEEE1588
- Double module, full size per AMC.0 and MTCA.4
- 1GbE base switch with dual 100/1000/10G uplink
- Full Layer 3 managed Ethernet switch
- Unified 1 GHz quad-core CPU for MicroTCA Carrier Management Controller (MCMC), Shelf Manager, Clocking, and Fabric management
- Automatic fail-over with redundant UTC006s

Benefits

- FPGA fabric option supports arbitrary scatter/gather or shelf-level signal processing
- Front-panel fabric expansion uses standard industry cables with copper or fiber options
- Sophisticated clocking features enabling GPS/IEEE1588/SyncE/NTP Grand Master Clock
- Virtual JTAG capability for remote programming and debugging eases FPGA code development
- VadaTech's Scorpionware® Shelf Management Software included at no additional cost

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UTC006

The VadaTech UTC006 is a double module (MTCA.4 format) MCH with front-panel fabric expansion and RTM support (PCIe option only). Fabric options include PCIe Gen3, 10/40GbE, Xilinx Virtex-7 FPGA, Cross Bar Switch (CBS), and SRIO.

The MCMC manages the Power Modules, Cooling Units, and up to 12 AMCs within the chassis. It also manages the fabric switch as well as the standard GbE with 10GbE uplink Base Channel switch.

The Ethernet switch is managed with an enterprise grade Layer 3 switching/routing stack and they support Synchronous Ethernet. The firmware in the UTC006 is HPM.2 compliant which allows for easy upgrades.

The unit provides Master JTAG services to the AMCs via the JSM, with an option for virtual JTAG capability.

The MCH has advanced clocking features including grand master clock and high-quality clock distribution/synthesis.

Figure 1: UTC006, PCIe Option

Figure 2: UTC006, FPGA Option

Figure 3: UTC006, 40GbE Option

Figure 4: UTC006, 10GbE Option

Block Diagram

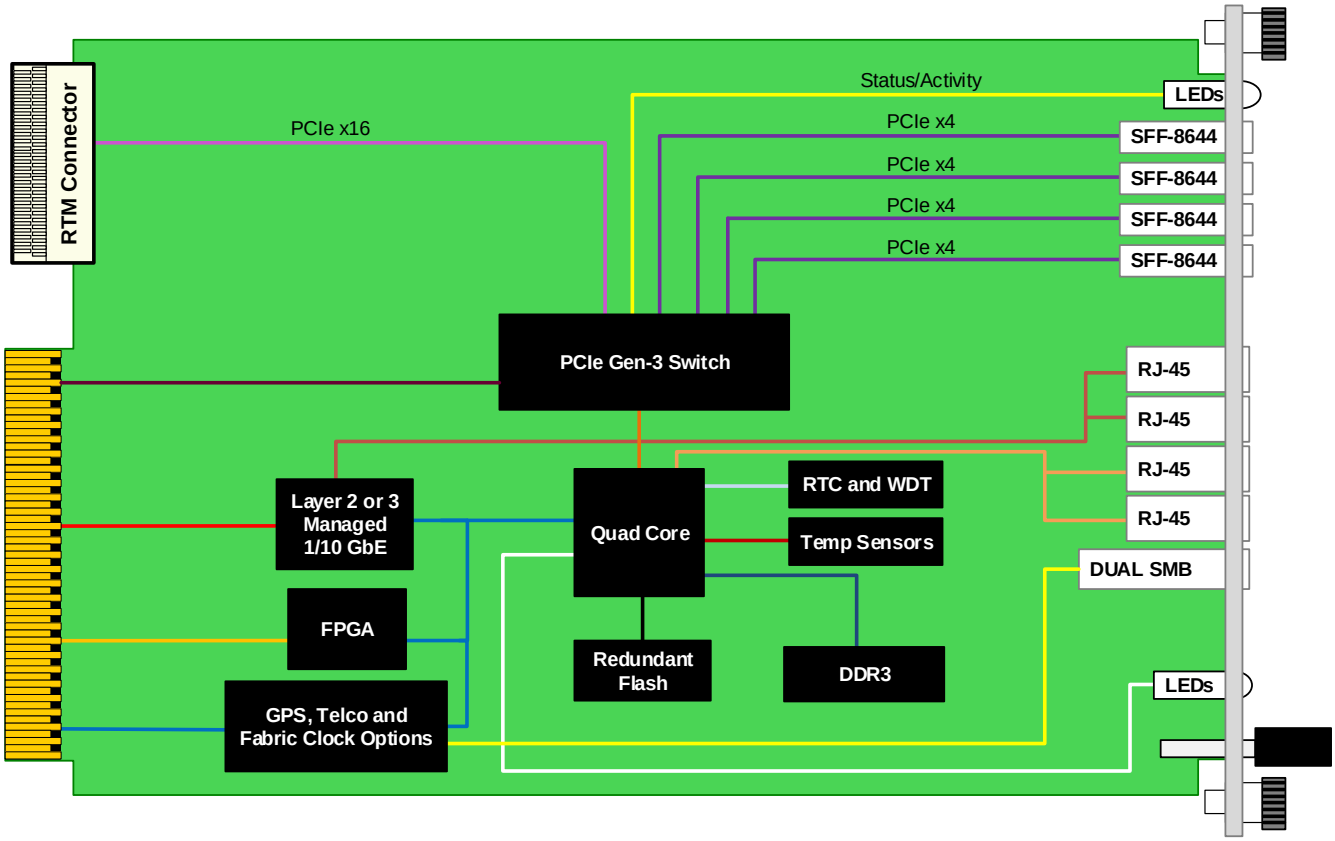

Figure 5: Block Diagram (PCIe Option)

Front Panel

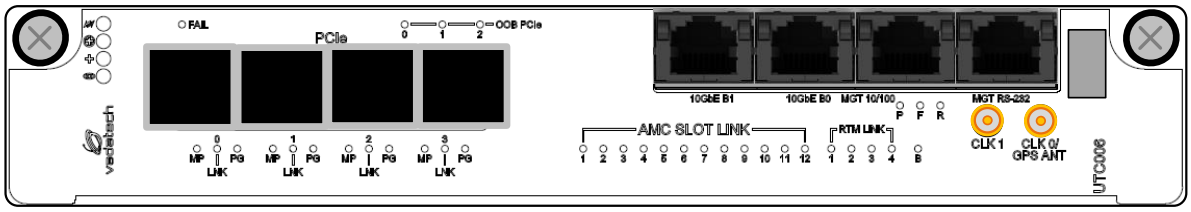

Figure 6: UTC006 Front Panel, PCIe Option

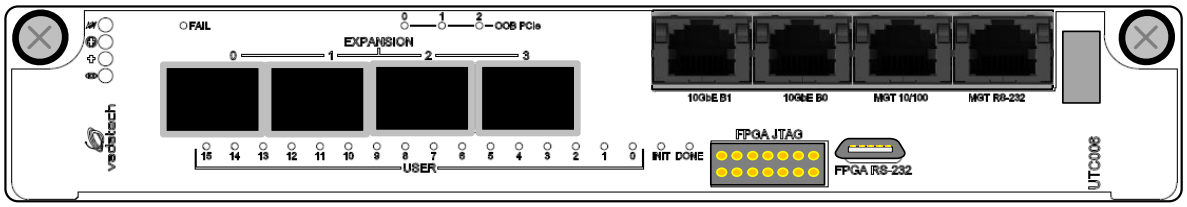

Figure 7: UTC006 Front Panel, FPGA Option

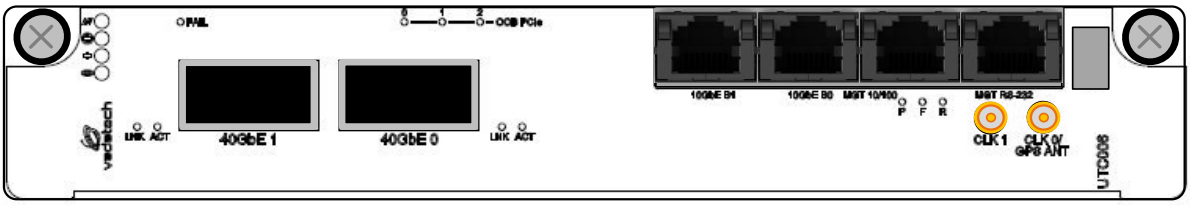

Figure 8: UTC006 Front Panel, 40GbE Option

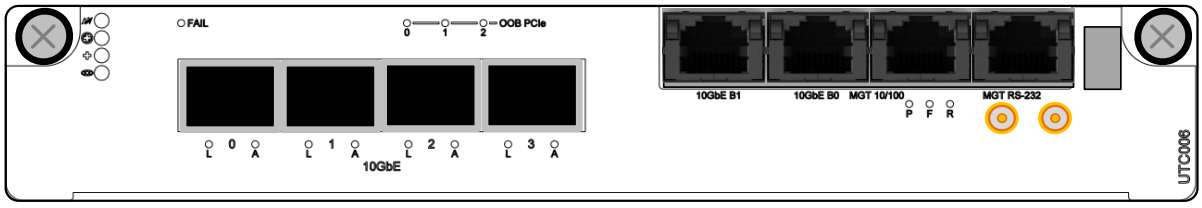

Figure 9: UTC006 Front Panel, 10GbE Option

Fabric Variations and General Connectivity

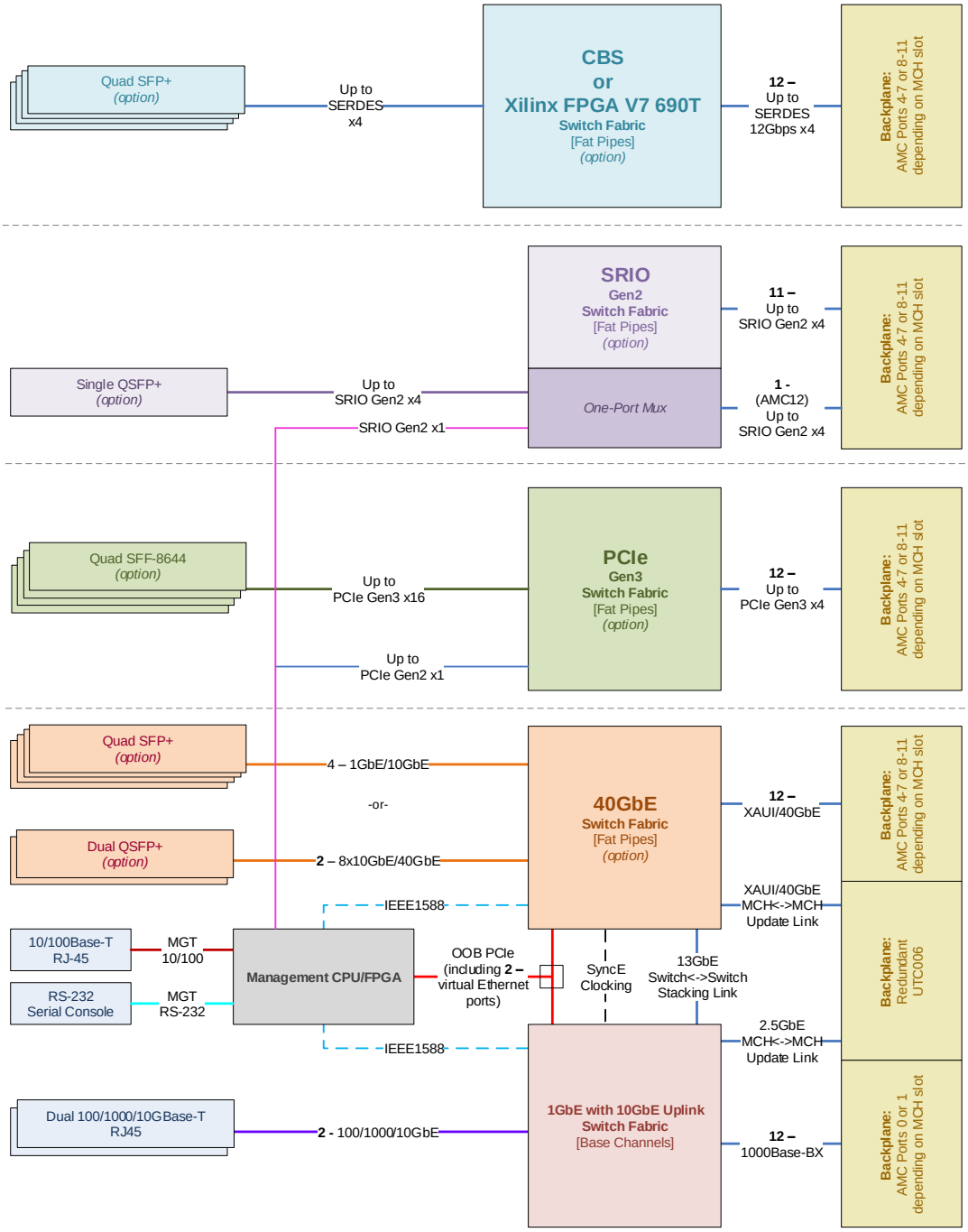

Figure 10: Block Diagram - Connectivity and Fabric Options

Architecture

IPMI Carrier Manager, Shelf Manager and Protocol Analyzer

The UTC006 utilizes the same proven standards-compliant IPMI management stack that has been utilized successfully in our previous generation MCH products. It supports carrier manager, shelf manager, and protocol analyzer operations to help facilitate a seamless chassis integration experience. The IPMI stack enables a rich feature set including:

- IPMI v2.0 with IPMI v1.5 compatibility
- SDR, FRU, and SEL storage interfaces (SEL stored in MRAM for high-speed/non-volatile/no-wear-out access)
- Intelligent temperature, voltage, and current sensing
- Shelf cooling policy
- Shelf activation and power management/Automatic fail-over/redundancy management
- Alarm controls
- Event notification and flexible alerting policies
- Backplane E-Keying
- CLI, SNMP, RMCP+, HTTP, and HPI
- IPMB Protocol Analyzer GUI for use on PC
- ScorpionWare GUI system manager integration tool on PC available separately

Base Channel Ethernet Switch

The UTC006 provides includes as standard a GbE base channel switch which includes two 10GbE uplink 100/1000/10G RJ-45 Ports. This switch is fully Layer 2 or Layer 3 managed enabling a comprehensive enterprise-grade routing and switching feature set. It supports Synchronous Ethernet (SyncE) and IEEE1588.

Fat Pipe Fabrics

The UTC006 provides for PCIe fat pipes fabric options:

PCIe Gen3 Switch with front QSFP+ expansion/uplink ports

- Speed setting for 2.5/5/8 Gbps per lane
- Virtual Switch/Multiple domain/Non-transparent port support to enable partitioning of the system with multiple root complexes
- Includes an extra internal port which enables the GPS precision time-stamping engine (accessible from an AMC root complex board)
- 1024 Gbps aggregate bandwidth/non-blocking/cut-through architecture

40GbE Switch with front single QSFP+ or dual SFP+ or dual 100/1000/10G RJ-45 expansion/uplink ports

- Full Layer 2 or 3 management enabling enterprise-grade switching and routing
- Supports Synchronous Ethernet (SyncE) and IEEE1588 to facilitate advanced system synchronization via Ethernet
- 320 Gbps or 640 Gbps aggregate bandwidth options for mixed 10GbE/40GbE and full 40GbE port configurations

SRIO Gen2 x4 Switch with front QSFP+ expansion/uplink port

- Supports 1.25/2.5/3.125/5/6.25 Gbps per lane
- 240 Gbps aggregate bandwidth/non-blocking/cut-through architecture

Cross-Bar Switch with front QSFP+ expansion/uplink port

- Supports unicasting or multi-casting of any input SERDES lane to one or more output SERDES lane
- 771 Gbps aggregate bandwidth/asynchronous/non-blocking architecture passes through any data rate up to 10.709 Gbps
- SERDES protocol agnostic (no packet framing/handling within the switch, only the AMCs need to understand the protocol)

Xilinx 690T FPDA

- Support for any protocol defined by user
- x4 lanes to each of the AMC modules

Fabric Clock Option

The UTC006 has the capability to provide a 100 MHz HCSL PCIe Gen3 compliant fabric clock to each AMC. This option enables the recommended synchronous PCIe clocking approach within the chassis when used in combination with the PCIe fabric.

GPS and General-Purpose Clocks

The MTCA specification defines a set of clocks for telecom and non-telecom applications. The VadaTech UTC006 has the most sophisticated clocking distribution in the market to meet the most stringent requirements such as wireless infrastructure, high speed A/D, etc. The UTC006 supports the following GPS and general-purpose clocking features:

- MTCA.4-compliant low-jitter/low-skew backplane crossbar clock routing matrix for CLK1/CLK2/CLK3 for all AMCs
- Clock disciplining with arbitrary clock frequency output and holdover (Stratum-3 option) including 1PPS regeneration and holdover
- Flexible integration and synchronization between GPS, IEEE1588/SyncE, and NTP clocking enabling Grand Master clock functionality
- 'Any Frequency' high-quality clock generation/jitter cleaning for up to two user clocks
- Supports hitless automatic clock failover for improved reliability
- Optional built-in GPS receiver enables direct time/clock synchronization to the GPS satellite constellation

The UTC006 supports flexible front panel clock port ordering options:

- Two DC-coupled LVCMOS Inputs/Outputs, or two AC-coupled Sine-wave Inputs, or one of each
- Built-in GPS receiver for time/location/clock synchronization plus a DC-coupled LVCMOS Input/Output

GPS Receiver Enabled Features

The UTC006 can be ordered with a GPS Receiver option. The receiver disciplines an onboard high-quality DPLL which is phase/frequency aligned to the atomic clocks in the GPS satellite constellation. The onboard clock synthesis/jitter cleaning capability can be utilized to convert this frequency into any frequency desired while still remaining locked to the GPS atomic clocks.

When the GPS Receiver option is purchased the UTC006 has the capability to re-transmit the incoming GPS data via Ethernet to other nodes in the network in the Trimble TSIP binary protocol format. This GPS data is also sent out the front panel GPS RS-232 serial port in the standard NMEA format for use by external equipment. When the GPS Receiver option is purchased along with the PCIe Fat Pipes fabric, the MCH also provides a precision PCIe Timestamping Engine capability to a PrAMC PCIe Root Complex on the backplane. This engine appears as a PCIe device to the AMC card and a device driver is available which will allow the AMC card to read all GPS status including position, velocity, status, etc., in addition to precision timestamps, time trigger, and time event interrupt functionalities.

IEEE1588 PTP AND NTP Grand Master Clock

The UTC006 can provide Ethernet time services to the chassis networks on both the GbE and 40GbE fabric ports. It can be subordinate to an external PTP or NTP master server or when the GPS receiver option is purchased can act as a Grand Master clock utilizing the precision timing information provided via the GPS receiver and onboard disciplined oscillator.

Synchronous Ethernet

The UTC006 provides a Synchronous Ethernet (SyncE) on the GbE and 40GbE fabric ports. With this feature, ports on the 1G and/or 40G Ethernet switches can be designated as master or slave ports and the Ethernet fabrics within the chassis can be synchronized from end-to-end with external equipment. This feature utilizes advanced telecom-grade network synchronization PLLs to provide exceptional SyncE performance.

JTAG Master/JTAG via Ethernet Virtual Probe

The UTC006 provide JTAG Master Capability to send out configuration data streams via the chassis JTAG Switch Module (JSM) to configure arbitrary JTAG Slave devices on AMC cards. Virtual Probe services are also available to provide JTAG via Ethernet for Xilinx FPGAs. This allows for standard development tools such as Xilinx iMPACT/ChipScope to treat the MCH/JSM combination as if it was a standard JTAG probe. This approach frees the developer from having to attach JTAG probes directly to the AMC or JSM which can be difficult when systems are already fully assembled. It also allows for remote debugging across long distances when required without the need to install additional JTAG equipment on-site.

Specifications

Architecture		
Physical	**Dimensions**	Double module, full-size
		Width: 5.85” (148.5 mm)
		Depth 7.11” (180.6 mm)
Type	**Controller**	MicroTCA Carrier Hub
Standards		
MTCA	**Type**	MTCA.0 Revision 1, MTCA.1 and MTCA.4
AMC	**Type**	AMC.0, AMC.2, AMC.3 and/or AMC.4
Module Management	**IPMI**	IPMI v2.0
		HPM v1.0
ATCA	**Type**	PICMG 3.0 Revision 2.0
Configuration		
Power	**UTC006**	Option load dependent (as the MCMC and Shelf only < 4W, up to 80W)
Environmental	**Temperature**	See Ordering Options
		Storage Temperature: –40° to +85°C
	Vibration	Operating 9.8 m/s^2 (1G), 5 to 500 Hz on each axis
	Shock	30Gs each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	**Interface Connectors**	RS-232 serial console port (RJ-45) and option for GPS NMEA serial data in/out
		Out-of-band LAN 10/100 from MCMC/Shelf Manager (RJ-45)
		Two in-band 100/1000/10G from Base Switch Fabric (RJ-45)
		Two CLK IN/OUT (SMB); CLK IN becomes GPS ANT IN with GPS receiver option
		Quad SFF-8644 for PCIe Gen 3 expansion
	LEDs	IPMI management control
		LNK/ACT, OOB PCIe error, ACTIVE MCMC, GPS receiver status, Clock: Ref Good, Freq Lock, Phase Lock, additional LEDs per each fat pipes fabric type
	Mechanical	Hot-swap ejector handle
Software Support	**Operating System**	Linux and Windows
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

UTC006 – AB0-DEF-GHJ

A = Fabric	D = Front Panel Clocking*1	G = JTAG Virtual Probe
0 = PCIe Gen3 1 = Xilinx V7 690T FPGA (Speed -2) 2 = Cross Bar Switch (CBS) 3 = 10GbE 4 = 40GbE (320 Gbps 10GbE/40GbE) 5 = 40GbE (full 40GbE) 6 = SRIO 7 = No Fabric (GbE on the base board only)	0 = No FP clocking (Backplane clocking only) 1 = Dual LVCMOS Clock In/Out 2 = Sine Wave In + LVCMOS In/Out 3 = Built-in GPS receiver + LVCMOS In/Out 4 = Dual Sine Wave In 5 = GPS receiver + Sine Wave In 6 = Sine Wave In (up to 17dBm) +TTL/LVCMOS In	0 = No JTAG Virtual Probe 1 = JTAG Virtual Probe Included
B = Included Transceiver Modules for Fabric Switch	**E = Fabric B Ports Configuration*3**	**H = MicroTCA Form Factor**
0 = No TXCVR 1 = SFP+ modules (10GBASE-SR)*4 2 = SFP+ modules (10GBASE-LR)*4 3 = SFP+ modules (1Gb LC/SX)*4 4 = SFP+ modules (1Gb LC/LX)*4 5 = SFP+ modules (1000Base-T)*4 6 = QSFP+ modules (SR)*4 7 = QSFP+ modules (LR)*4	0 = Fixed 100 MHz HCSL fabric clock for PCIe routed to backplane CLK3/FCLKA channels 1 = General-purpose M-LVDS clock matrix routed to backplane CLK3/FCLKA channels	0 = MTCA.0 (Base specification, Air-cooled) 1 = MTCA.1 (Rugged, Air-cooled)
	F = Clock Holdover Stability	**J = Temperature Range and Coating**
	0 = Standard (XO) 1 = Stratum-3 (TCXO) 2 = Stratum-3 (OCXO)	0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40 to +85°C), Humiseal 1A33 Polyurethane*2 7 = Extended (–40 to +85°C), 1B31 Acrylic*2

Notes:

***1** Backplane M-LVDS clock routing and related PLL clocking features are provided regardless of the front panel clock option. When GPS (D=3) is selected, additional GPS-related features become available such as precision GPS time-stamping via PCIe, GPS data transmission via Ethernet, and GPS serial NMEA data 'Y' cable is provided.

***2** Conduction cooled; temperature is at edge of module. Consult factory for availability.

***3** E=0 is recommended for PCIe fabric applications. These options correspond with the MCH backplane connector pin-out variations described in the MTCA standard.

***4** This option is only applicable when selecting the 10/40GbE, CBS or the FPGA in Option "A".

Related Products

VT815

- MTCA Chassis Platform with rear I/O 19” x 9U x 14.9” deep (with handles 16.23” deep)
- Full redundancy with dual MicroTCA Carrier Hubs (MCH), dual cooling units and 3 PSUs
- Up to twelve AMCs: 12 full-size double modules

DAQ523

- Complete Data Acquisition sub-system
- Supported by DAQ Series™ data acquisition software
- Twelve channel ADC 16-bit @ 125 MSPS (AD9653)

AMC726

- Intel® 4th Gen Core i7-4700EQ with QM87 chipset
- PCIe Gen3 x4 on Ports 4-7 and 8-11 or single PCIe x8 on Ports 4-11 (AMC.1)
- Serial over LAN

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