

VPX007

24 x 10GbE Switch with Optional Health Management, 6U VPX



VPX007

Key Features

- Versatile Layer 2 managed Ethernet switch
- Total of 24 Ports of 10GbE
- Up to eight SFP+ Ports on the front panel
- Unified 1 GHz quad-core CPU for Shelf Manager, and Fabric management
- Automatic fail-over with redundant VPX007
- Frequency disciplined to GPS/SyncE (Slave the SyncE)
- VITA 46 and VITA 65 compliant

Benefits

- Optional sophisticated clocking features enabling GPS/SyncE/NTP Grand Master Clock
- Optional virtual JTAG capability for remote programming and debugging eases FPGA code development
- VadaTech's Scorpionware® Shelf Management Software included at no additional cost
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™



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VPX007

The VadaTech VPX007 is a versatile 10GbE VPX switch with optional Tier-2 support for health management and features a total of 24 Ports of 10GbE. The unit can be configured to have all 10GbE Ports routed to the front panel with P1, P2, P3 and P4 unpopulated, or to have 10GbE Ports routed to the backplane as well as the front panel. The board provides up to a total of x16 10GbE as XAU1 to the backplane (x4 10GbE going to each of P1/P2/P3/P4).

The optional health management uses software based on VadaTech's robust Carrier Manager and Shelf Manager which have been deployed for years with proven results. The Module can also run as the shelf manager within the system.

The MCMC manages the Power Modules, Cooling Units, and up to 12 payload modules within the chassis.

The Ethernet switch is managed with an enterprise grade Layer 2 switching/routing stack which supports Synchronous Ethernet.

The unit runs Linux on its centralized quad-core CPU and is fully redundant when used in conjunction with a second instance of the module. The firmware is HPM.2 compliant which allows for easy upgrades.

VPX007 provides Master JTAG services to the payload modules via the JSM and has advanced clocking features including grand master clock and high-quality clock distribution/synthesis.

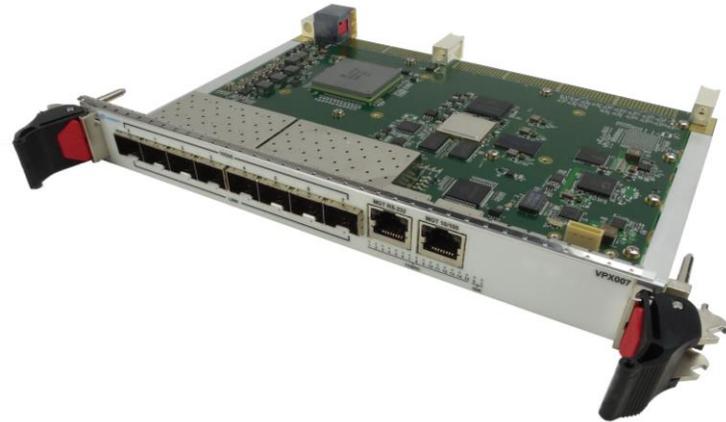


Figure 1: VPX007

Block Diagram

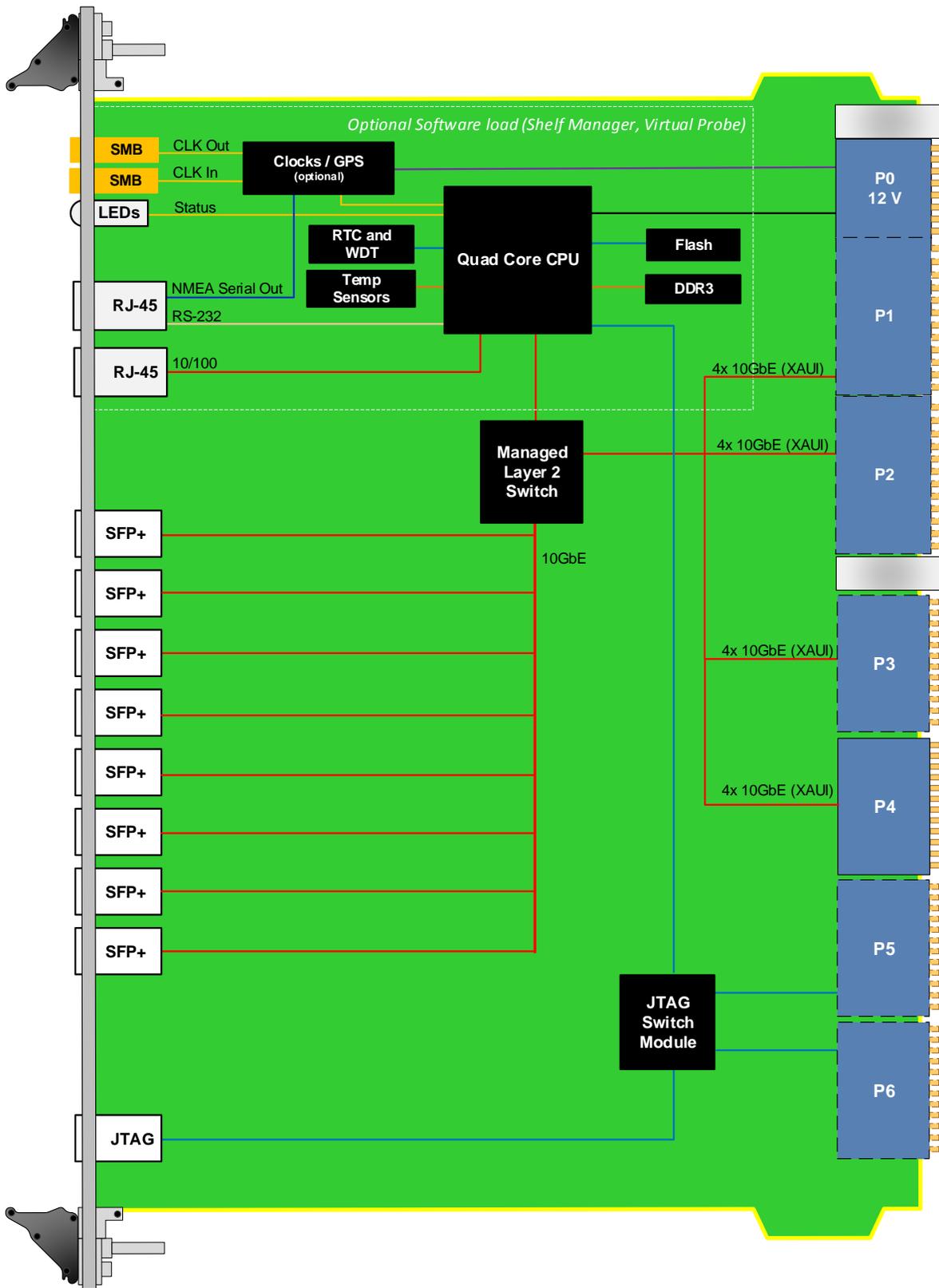


Figure 2: VPX007 Functional Block Diagram

Architecture

Optional IPMI Carrier Manager, Shelf Manager and Protocol Analyzer

The VPX007 utilizes the same proven standards-compliant IPMI management stack that has been utilized successfully in our previous generation products. It supports carrier manager, shelf manager, and protocol analyzer operations to help facilitate a seamless chassis integration experience. The IPMI stack enables a rich feature set including:

- IPMI v2.0 with IPMI v1.5 compatibility
- SDR, FRU, and SEL storage interfaces (SEL stored in MRAM for high-speed/non-volatile/no-wear-out access)
- Intelligent temperature, voltage, and current sensing
- Shelf cooling policy
- Shelf activation and power management/Automatic fail-over/redundancy management
- Alarm controls
- Event notification and flexible alerting policies
- CLI, SNMP, RMCP+, HTTP, and HPI
- IPMB Protocol Analyzer GUI for use on PC
- ScorpionWare GUI system manager integration tool on PC (available separately)

Fat Pipe Fabric

The VPX007 10GbE Switch provides:

- Layer 2 management
- SyncE Grand Master based on GPS (it cannot discipline to SyncE from another Master)
- 240 Gbps aggregate bandwidth

GPS and General-Purpose Clocks

The VadaTech VPX007 has the most sophisticated clocking distribution in the market to meet the most stringent requirements such as wireless infrastructure, high speed A/D, etc. The VPX007 supports the following GPS and general-purpose clocking features:

- Low-jitter/low-skew backplane routing
- Clock disciplining with arbitrary clock frequency output and holdover (Stratum-3 option) including 1PPS regeneration and holdover
- Flexible integration and synchronization between GPS, SyncE, and NTP clocking enabling Grand Master clock functionality
- 'Any Frequency' high-quality clock generation/jitter cleaning for up to two user clocks
- Hitless automatic clock failover for improved reliability
- Optional built-in GPS receiver enables direct time/clock synchronization to the GPS satellite constellation

The VPX007 supports flexible front panel clock port ordering options:

- Two DC-coupled LVCMOS Inputs/Outputs, or two AC-coupled Sine-wave Inputs, or one of each
- Built-in GPS receiver for time/location/clock synchronization plus a DC-coupled LVCMOS Input/Output

GPS Receiver Enabled Features

The VPX007 can be ordered with a GPS Receiver option. The receiver disciplines an onboard high-quality DPLL which is phase/frequency aligned to the atomic clocks in the GPS satellite constellation. The onboard clock synthesis/jitter cleaning capability can be utilized to convert this frequency into any frequency desired while still remaining locked to the GPS atomic clocks.

When the GPS Receiver option is purchased the VPX007 has the capability to re-transmit the incoming GPS data via Ethernet to other network nodes in the Trimble TSIP binary protocol format. This GPS data is also sent out the front panel GPS RS-232 serial port in the standard NMEA format for use by external equipment.

NTP Grand Master Clock

The VPX007 can provide Ethernet time services to the chassis networks on both the GbE and 10GbE fabric ports. It can be subordinate to an external NTP master server or when the GPS receiver option is purchased can act as a Grand Master clock utilizing the precision timing information provided via the GPS receiver and onboard disciplined oscillator.

Synchronous Ethernet

The VPX007 provides a Synchronous Ethernet (SyncE) on the 10GbE fabric ports. With this feature, ports on the Ethernet switch can be designated as master ports and the Ethernet fabrics within the chassis can be synchronized from end-to-end with external equipment. This feature utilizes advanced telecom-grade network synchronization PLLs to provide exceptional SyncE performance.

JTAG Master/JTAG via Ethernet Virtual Probe

The VPX007 provides optional JTAG Master Capability to send out configuration data streams via the chassis JTAG Switch Module (JSM) to configure arbitrary JTAG Slave devices on VPX cards. Virtual Probe services are also available to provide JTAG via Ethernet for Xilinx FPGAs. This allows for standard development tools such as Xilinx iMPACT/ChipScope to treat the switch/JSM combination as if it was a standard JTAG probe. This approach frees the developer from having to attach JTAG probes directly to the VPX or JSM which can be difficult when systems are already fully assembled. It also allows for remote debugging across long distances when required without the need to install additional JTAG equipment on-site.

Specifications

Architecture		
Physical	Dimensions	6U, 1" pitch
Type	Controller	OpenVPX Switch with optional Health Management
Standards		
VPX	Type	VITA 46.x
VPX	Type	VITA 65 OpenVPX
Module Management	IPMI	IPMI v2.0 HPM v1.0
Configuration		
Power	VPX007	Option load dependent (typical 35W) On P0; VS1 = 12V
Front Panel	Interface Connectors	10G over SFP+ CPU 10/100 (RJ-45) CPU RS-232 (RJ-45) Option for GPS NMEA serial data in/out (RJ-45) LEDs Status Two CLK IN/OUT (SMB); CLK IN becomes GPS ANT IN with GPS receiver option
VPX Interfaces	Slot Profiles Rear IO	See Ordering Options CPU on P0 Clocks/GPS (Optional) on P0 10GbE on P1/P2/P3 GbE on P2
Software Support	Operating System	Linux
Other		
MTBF		MIL Hand book 217-F@ TBD hrs
Certifications		Designed to meet FCC, CE and UL certifications, where applicable
Standards		VadaTech is certified to both the ISO9001:2015 and AS9100D standards
Warranty		Two (2) years, see VadaTech Terms and Conditions

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX007 – ABC-DEF-GHJ-K00

A = Fabric Routing (rear only) 0 = P1/P2/P3/P4 not loaded 1 = P1/P2/P3/P4 loaded 2 = P2 loaded* 3 = Reserved 4 = Reserved	D = Front Panel Clocking 0 = No FP clock 1 = Dual LVCMOS Clock In/Out 2 = Sine Wave In + LVCMOS In/Out 3 = Built-in GPS receiver + LVCMOS In/Out 4 = Dual Sine Wave In 5 = GPS receiver + Sine Wave In 6 = Sine Wave In (up to 17dBm) +TTL/LVCMOS In	G = Applicable Slot Profile 0 = 5 HP, VITA 46 1 = 5 HP, VITA 48.1	K = VPX Connector Type 0 = Standard 50u Gold Rugged 1 = KVPX Connectors
B = Health Management 0 = No Shelf manager 1 = Shelf manager	E = Clock Holdover Stability 0 = Standard (XO) 1 = Stratum-3 (TCXO)	H = Environmental See Environmental Specification	
C = SFP+ TXCVRs (8 off) 0 = No TXCVRs 1 = 10GBASE-SR 2 = 10GBASE-LR (1KM) 3 = 10GBASE-LR (10KM) 4 = Copper 1000Base-TX 5 = Copper 10GBase-T	F = JTAG and Virtual Probe 0 = No JTAG (P5/P6 not fitted) 1 = JSM only 2 = JSM and Virtual Probe	J = Conformal Coating 0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic	

Notes:

*For redundancy the P2 must be loaded and combined with the correct backplane routing.

Environmental Specification

Option H	Air Cooled			Conduction Cooled	
	H = 0	H = 1	H = 2	H = 3	H = 4
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes:

*Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX516



- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX518



- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Zynq-7000 FPGA in FFG-900 package (XC7Z100 or XC7Z045)
- High-performance clock jitter cleaner

VPX599



- 3U FPGA Dual DAC and dual ADC per VITA 46
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS

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