VPX102

3U VPX Carrier for XMC Modules

VPX102

Key Features

- Support for XMC modules
- x8/x4 SERDES from XMC to P1
- Comprehensive user I/O routing options per VITA 46.9
- Health Management processor
- ANSI/VITA 42.3 (XMC PCI Express)
- Support for PCIe Gen3 or non-PCIe based XMC
- Health Management through dedicated Processor

Benefits

- Most comprehensive XMC carrier on the market
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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The VPX102 is a carrier module (VITA 46). It provides PCIe Gen3 x8 and is the most comprehensive VPX carrier available for XMC modules.

The J14/J16 connector of the XMC are routed per VITA 46.9. The module supports different backplane pin field assignments to support rear I/O access for the XMC module. The following profiles are supported:

- P2w1-P64s (Figure 1)
- P1w9-X12d+P2w1-P64s (Figure 2)
- P2w7-X8d+X12d (Figure 3)
- P2w1-X24s+X8d+X12d (Figure 4)
- P2w3-X38s+X8d (Figure 5)
- P1w9-X12d+P2w3-X38s+X8d (Figure 6)
- P1w13-X38s+X8d+X12d (Figure 7)

The module supports PCIe and None-PCIe based XMC. The module has a re-timer onboard which allows the XMC to drive long traces on the backplane as well as cleaning the received data from long traces coming from the backplane to the XMC.

This modular approach allows a VPX carrier and VPX Chassis to utilize the large numbers of XMC modules available on the market.

Figure 1: VPX102 Front View

Block Diagram

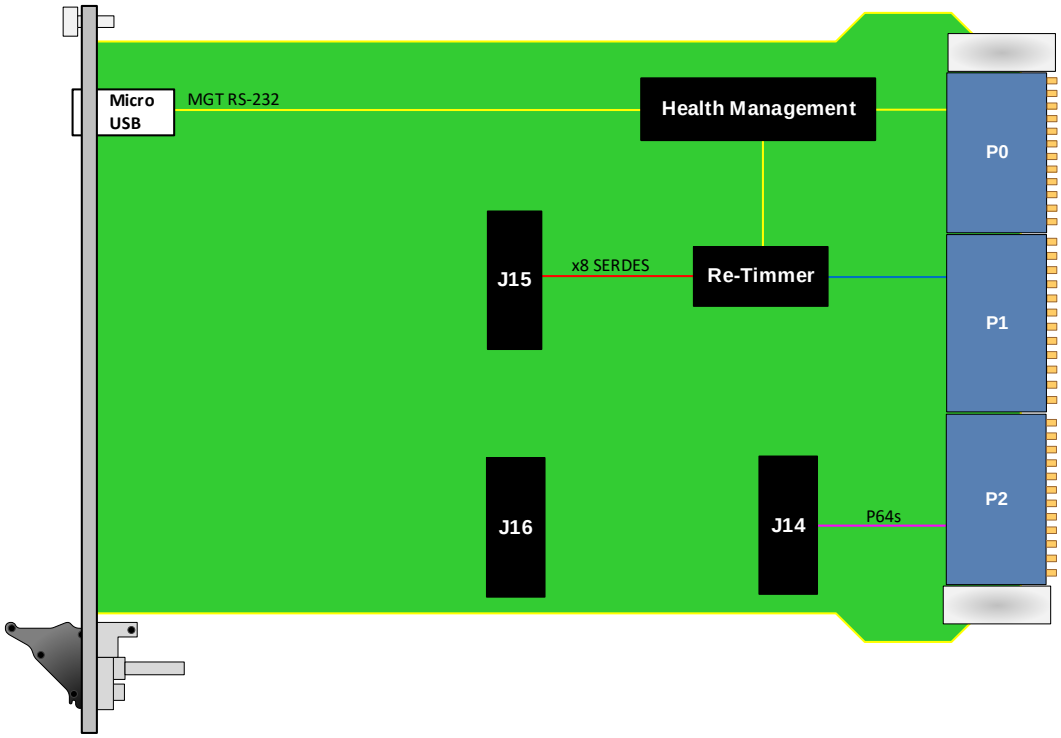

Figure 2: VPX102 Functional Block Diagram, Option D=0
(3U Carrier P64s Mapping)

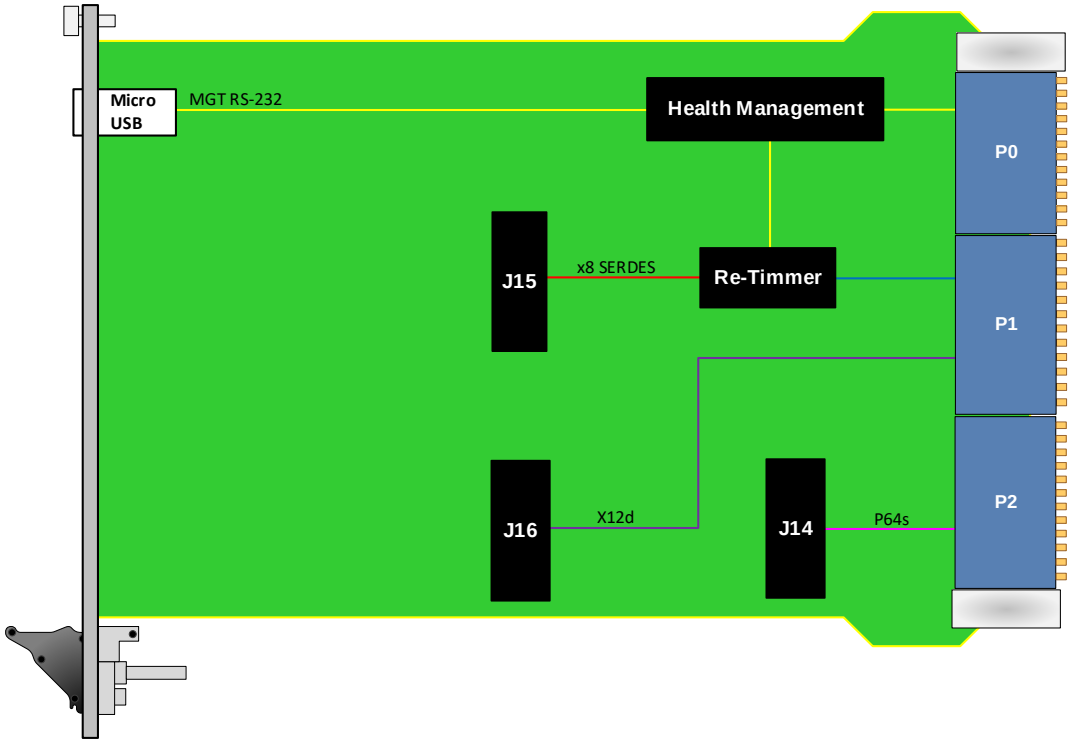

Figure 3: VPX102 Functional Block Diagram, Option D=1
(3U Carrier X12d+P64s Mapping)

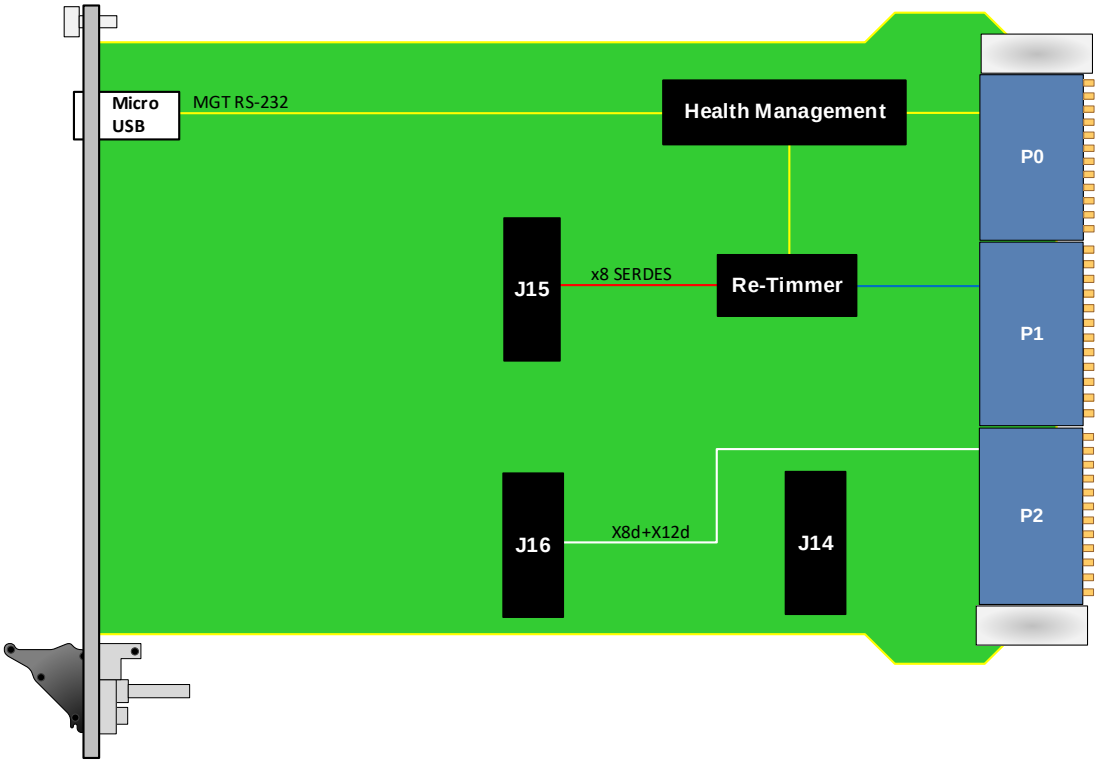

Figure 4: VPX102 Functional Block Diagram, Option D=2
(3U Carrier X8d+X12d Mapping)

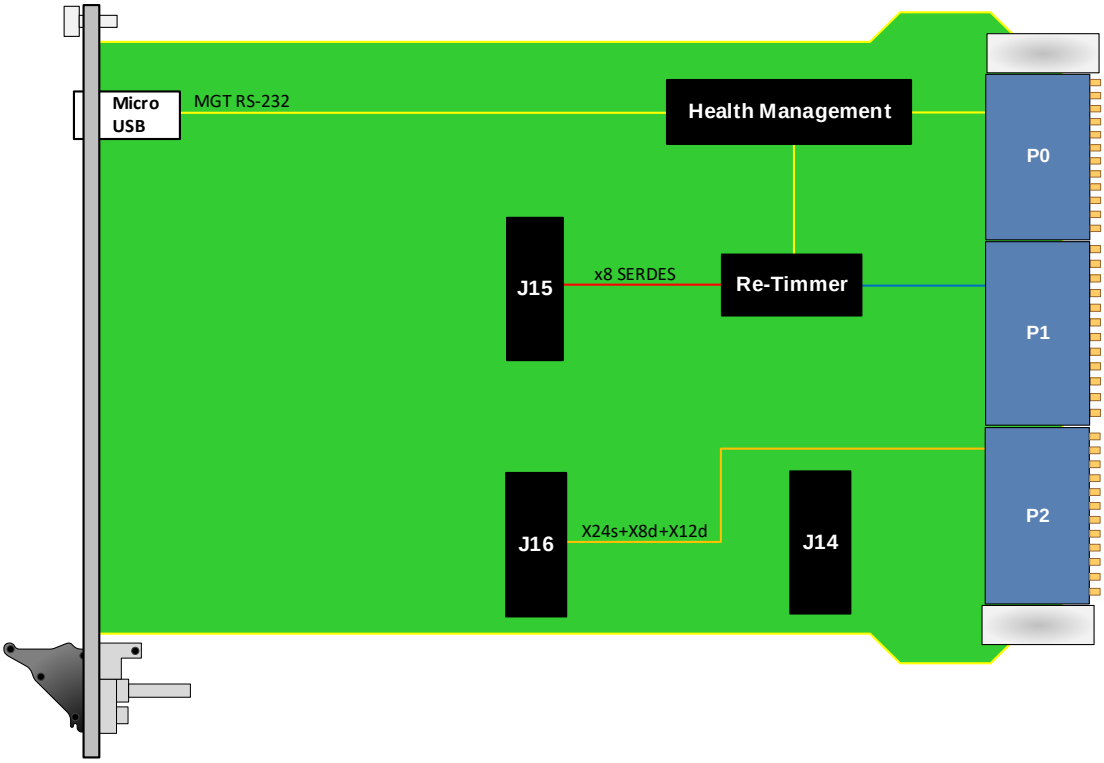

Figure 5: VPX102 Functional Block Diagram, Option D=3
(3U Carrier X24s+X8d+X12d Mapping)

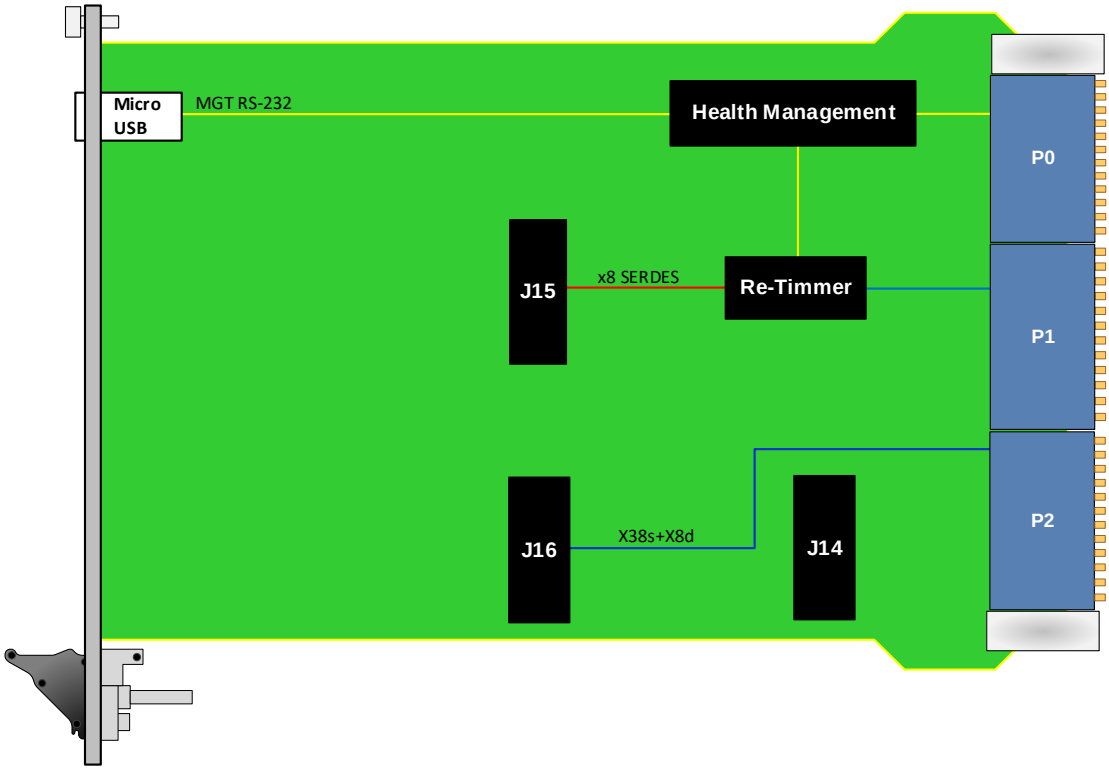

Figure 6: VPX102 Functional Block Diagram, Option D=4
(3U Carrier X38s+X8d Mapping)

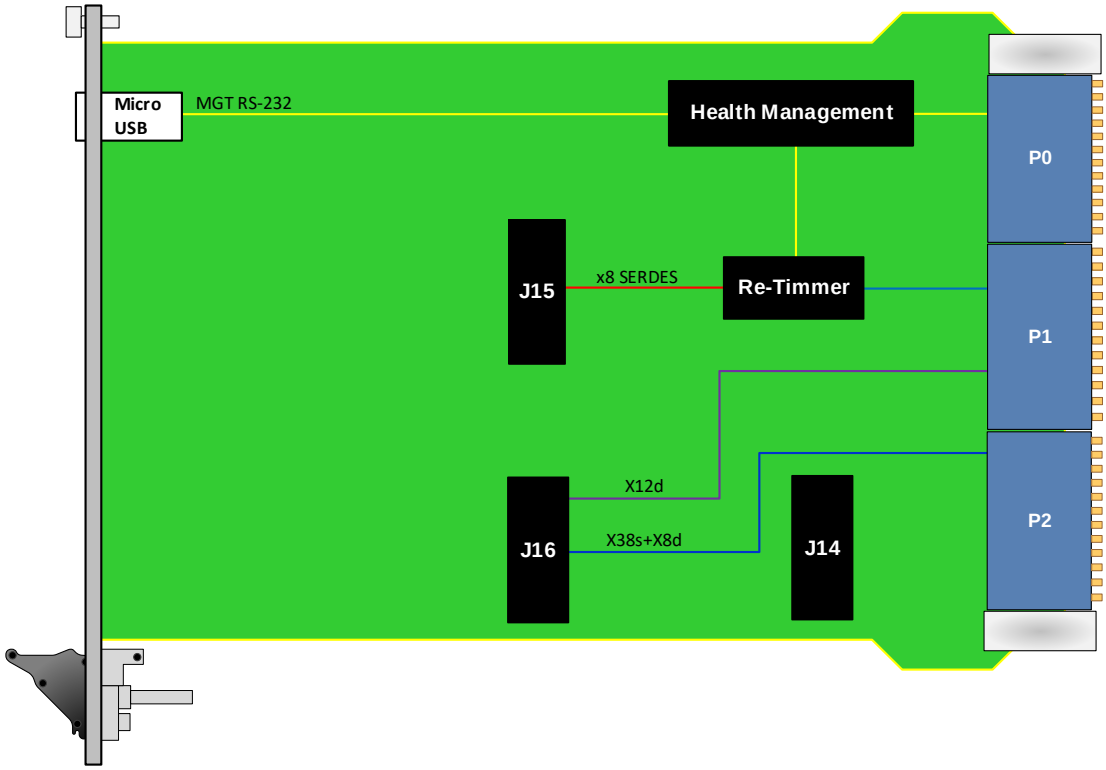

Figure 7: VPX102 Functional Block Diagram, Option D=5
(3U Carrier X12d+X38s+X8d Mapping)

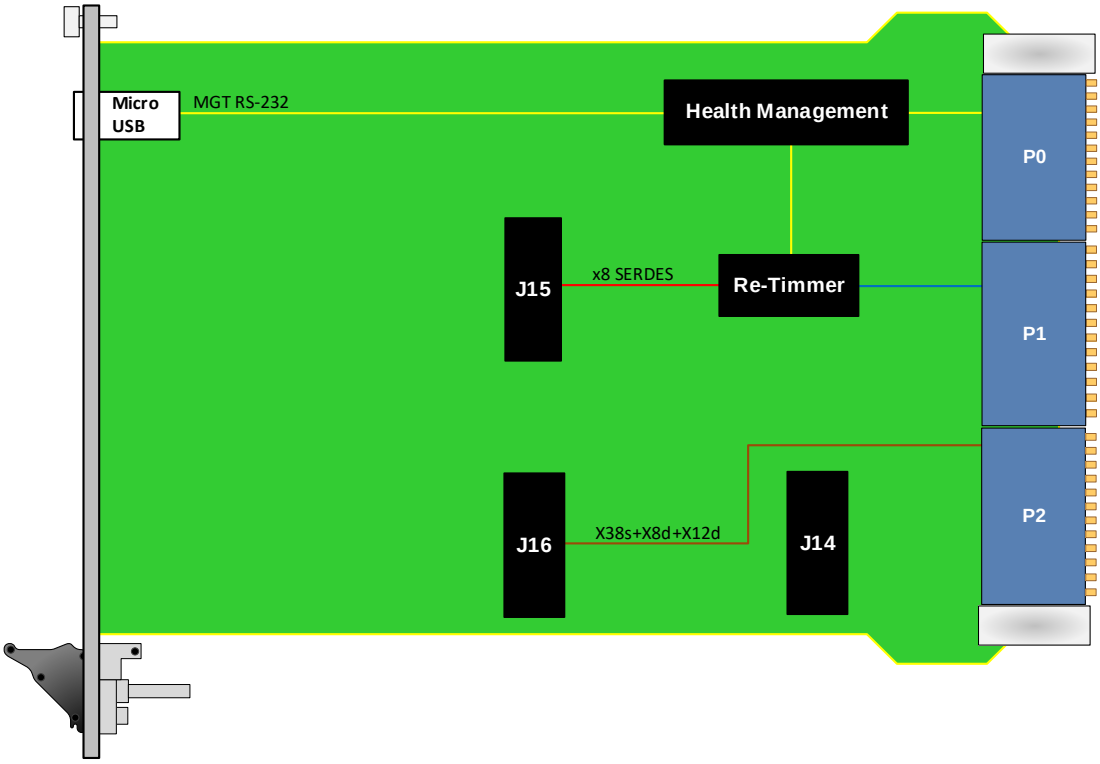

Figure 8: VPX102 Functional Block Diagram, Option D=6
(3U Carrier X38s+X8d+X12d Mapping)

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
Standards		
VPX	**Type**	VITA 46.x
VPX	**Type**	VITA 65 OpenVPX
Module Management	**IPMI**	IPMI v2.0
Configuration		
Power	**VPX102**	XMC module dependent (re-timer, etc. 1W)
Front Panel		XMC
	Micro USB	RS-232 for Health Management
	LEDs	User defined by Health Management
Onboard Interfaces		XMC site
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	Defined by VITA 46.9 profile
	Power Supplies	From P0
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX102 – ABC-DE0-0HJ

A = XMC VPWR*	D = VITA 46.9 Pin field	G = Applicable Slot Profile
0 = +12V 1 = +5V	0 = P2w1-P64s 1 = P1w9-X12d+P2w1-P64s 2 = P2w7-X8d+X12d 3 = P2w1-X24s+X8d+X12d 4 = P2w3-X38s+X8d 5 = P1w9-X12d+P2w3-X38s+X8d 6 = P1w13-X38s+X8d+X12d 7 = Reserved 8 = Reserved	0 = 5 HP, VITA 48.1 1 = Reserved
B = XMC Fabric	**E = XMC Connector**	**H = Environmental**
0 = PCIe 1 = Non-PCIe based	0 = VITA 42 1 = VITA 61	See Environmental Specification
C = VPX Connector Type		**J = Conformal Coating**
0 = Standard 50u Gold Rugged 1 = KVPX Connectors		0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Notes:
*Per VITA specification the XMC VPWR can be powered from +5V or +12V. Please consult the XMC module that will be used.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes:
*Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX516

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX592

- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

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