VPX400

Versal Prime FPGA FMC+ Carrier
3U VPX

VPX400

Key Features

- 3U VPX form factor
- AMD Versal Prime XCVM1802 FPGA
- Single FMC+ (VITA 57.4) site
- 8 GB of 64-bit wide DDR4 Memory Single Bank with ECC to the CPU
- 8 GB of 64-bit wide DDR4 Memory Single Bank to the Fabric
- Integrated 34Mb block RAM and 130Mb UltraRAM
- Health Management through dedicated Processor

Benefits

- FMC+
- Versal MPSoC
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX400

The VPX400 is a 3U VPX FPGA Carrier with single FMC+ (VITA 57.4) interface. The unit has an onboard, re-configurable FPGA which interfaces directly to the VPX P1/P2 connector and all FMC+ LA/HA/HB pairs (the module does not support HSPCe connector and has only 16 SERDES routed to the FMC+).

The FPGA interfaces to two DDR4 memory blocks (8GB of 64-bit wide with ECC to the Processor Subsystem and 8GB of 64-bit wide to the Fabric). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The VPX400 is based on AMD Versal Prime XCVM1802 MPSoC FPGA. The FPGA has 1968 DSP Slices and 1968k logic cells. The XCVM1802 includes Dual-core ARM application processor, dual-core ARM Cortex-R5F. The module has x8 SerDes routed to the P1 which could run any protocol such as PCIe, SRIO, Ethernet, Aurora, etc. The module has dual GbE that could run as 1000Base-T to the P2 or as 1000Base-X to the P1 (ports 15/16).

The module has onboard 64 GB of Flash, 128 MB of boot flash and an SD Card as an option.

Note: The +VADJ voltage of the VPX400 is set to +1.5V, please make sure the FMC/FMC+ module can handle +1.5V for its +VADJ. If utilizing a Vadatech FMC/FMC+ please contact Vadatech sales to confirm the +VADJ value of the FMC/FMC+ module.

Figure 1: VPX400

Block Diagram

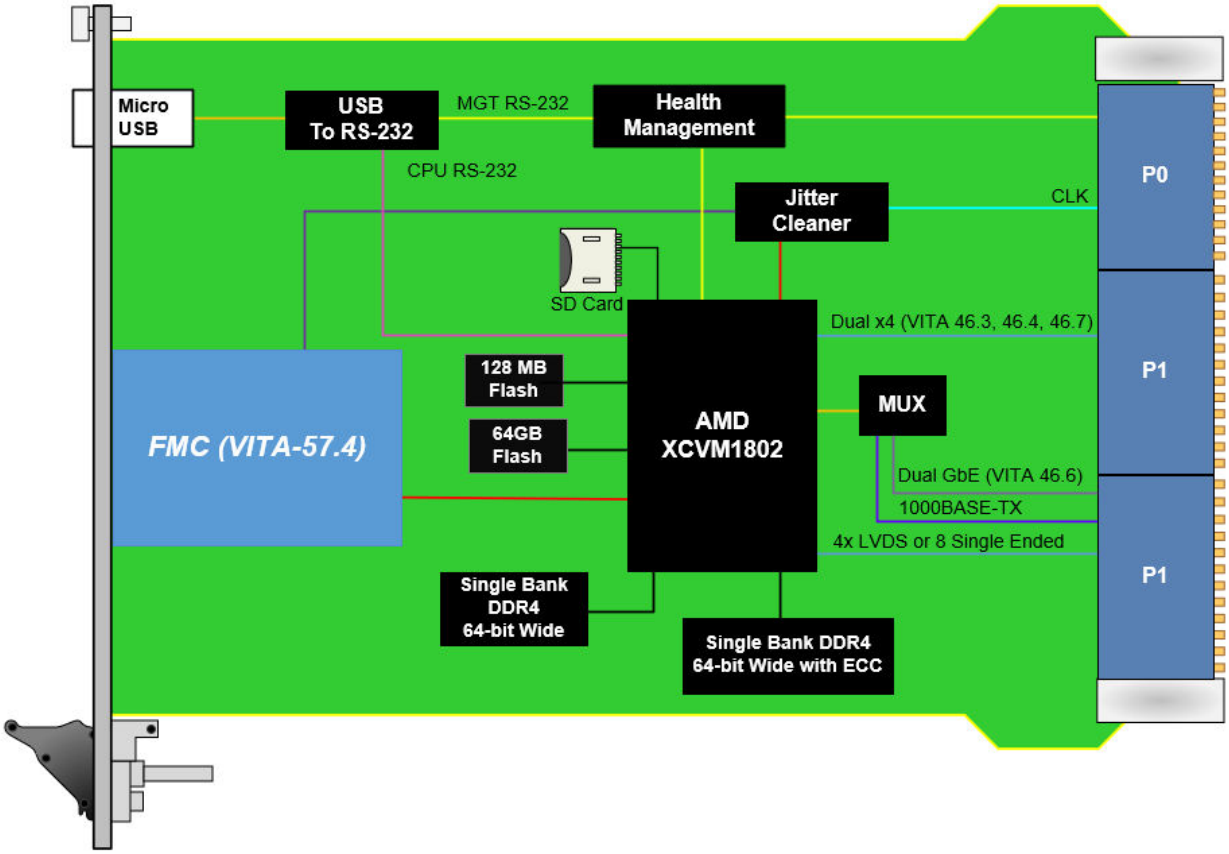

Figure 2: VPX400 Functional Block Diagram

Front Panel

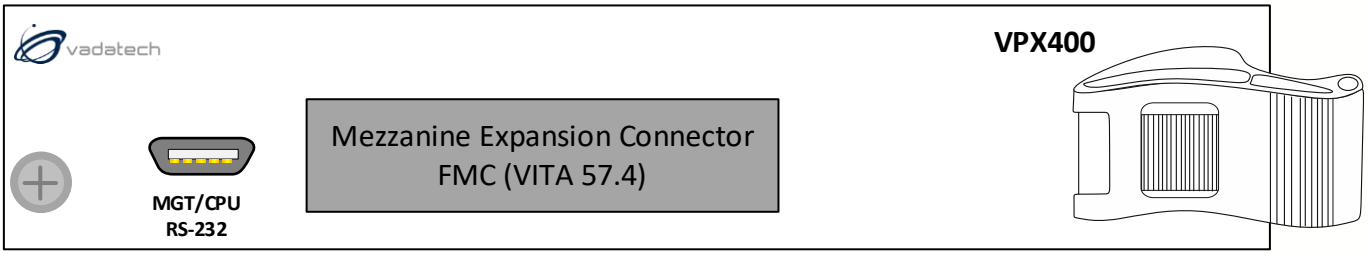

Figure 3: VPX400 Front Panel

Pinout Block Diagram

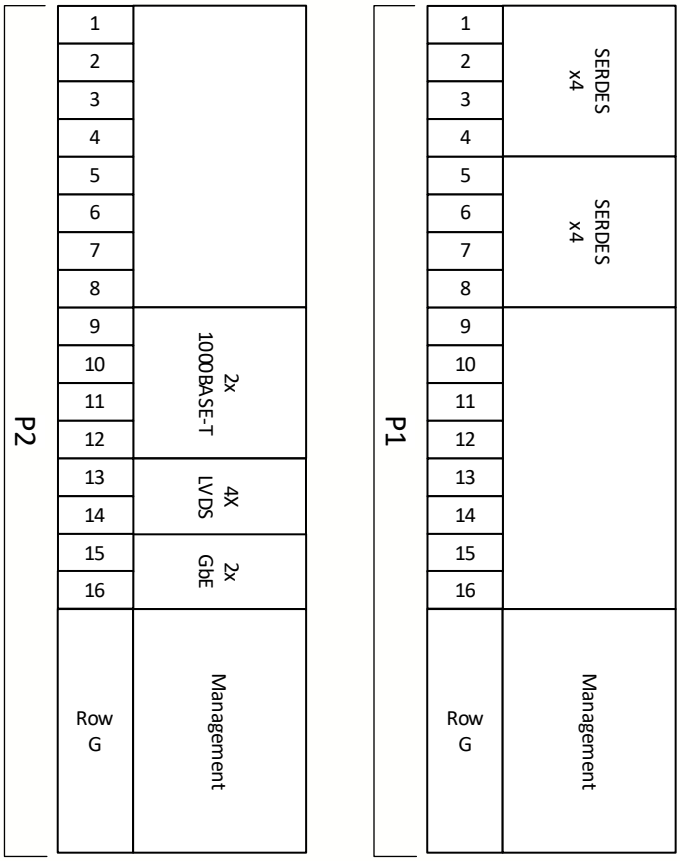

Figure 4: VPX400 P1/P2 Pinout Definition

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Reference Design

VadaTech provides an extensive range of AMD based FPGA products. The FPGA products are in two categories: FPGA boards with FMC carriers and FPGA products with high-speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

AMD provides Design Suite for developing applications on AMD based FPGAs. VadaTech provides reference VHDL developed using the AMD Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the AMD tool or AMD IP cores, so please contact AMD where these are required.

AMD also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

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Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
Type	**FPGA**	AMD Prime Versal with FMC+ site
Configuration		
Power	**VPX400**	~30W FPGA load dependent and no FMC+
Front Panel	**Interface Connectors**	Single FMC+ Slot
	Micro USB	RS-232 from Health Management and RS-232 from CPU via USB
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	P0: CLK
		P1: x8 SerDes (VITA 46.3, 46.4, 46.7, etc.)
		P2: GbE 1000BASE-T with 4 x LVDS
Software Support	**Operating System**	Linux or VxWorks
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

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Ordering Options

VPX400 – A0C-D0F-GHJ

A = VPX Connector Type	D = FPGA Speed	G = Applicable Slot Profiles
0 = Standard 50u Gold Rugged 1 = Reserved	1 = Reserved 2 = High 3 = Highest*	0 = 5 HP, VITA 48.1
		H = Environmental
		See Environmental Specification
C = SD Card	**F = PCIe Option (P1) for Data Port 1/2****	**J = Conformal Coating**
0 = No SD Card 1 = SD Card (64 GB)	0 = No PCIe (lanes 1 to 8) 1 = PCIe (lanes 1 to 4) 2 = PCIe (lanes 1 to 8)	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic 3 = Parylene

Notes:

* MOQ required

**When the Ports are not PCIe the lanes are electrically compatible with SRIO, XAUI, and other SerDes protocols.

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes:

*Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX401

- 3U FPGA carrier
- AMD
- High-performance clock jitter cleaner

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