VPX540

20 ADC 14-bit @ 4 GSPS with 16 DAC 14-bit @ 12 GSPS with Intel Agilex-9 SoC, 6U VPX

VPX540

Key Features

- Utilizing Intel Agilex SoC (AGRM027) with quad Core ARM Coretex-A53 in 6U VPX form factor
- 20 ADC 14-bit @ 4 GSPS and 16 DAC 14-bit @ 12 GSPS
- Low Latency ADC/DAC turn around
- 7.125GHz front end RF input/output Band-Width (BW)
- Direct to RF from Base-Band, L-Band, S-Band, C-Band
- 64GB File System
- 2x 128MB Boot Flash
- 4GB of DDR-4 (32-bit) with ECC to the HPS
- Three banks of 8GB of DDR-4 (64-bit wide) with ECC to the FPGA for total of 24GB
- Health Management through dedicated Processor per VITA 46.11 Tier-2 support

Benefits

- Integrated SoC provides RF/FPGA with large internal memory on a single device
- Reference design with VHDL source code speeds application development
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™

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VPX540

The VPX540 provides 20 ADC @ 4GSPS with 16 DAC @ 12GSPS with 14-bit resolution with integrated FPGA and quad Core ARM Cortex-A53 as a System on Chip (SoC). The ADC/DAC have a front-end RF bandwidth of 7.125 GHz. The module has 24GB of the DDR-4 memory to the FPGA as three banks of 8GB 64-bit wide each with the ECC. To the ARM there is single bank of 4GB of 32-bit wide DDR-4 memory with ECC.

The FPGA interfaces directly to rear I/O via high-speed SERDES, supporting PCIe, SRIO, Ethernet (1G/10G/25G/50G/100G/200G/400G), and/or Serial Lite backplane connections. General purpose I/O signals and LVDS are also routed to the rear. The front panel contains a total of 12 status and user-defined LEDs. All the RF connections are thru the front panel via SSMC (38 total). The module's front panel also has a QSFP-DD (Quad Small Form Factor Pluggable Double Density) egress port which can go up to 400G.

The on-board PLL can lock into the incoming clock for synchronizing to an external clock and provides synchronized clocks to the ADC/DAC for the RF sampling. The sampling on the ADC/DAC are fully coherent with each other.

The module has capability to synchronize across multiple modules within the chassis. This allows digital beam forming for phased array radar. The module could be used for other applications such as SAR (Synthetic Aperture Radar), EW/ECM Jamming, Military Communication System as well as Military COTS Digitizer.

The VPX540 includes platform health management/monitoring capability using VadaTech's field-proven IPMI software as Tier-2 support per VITA 46.11.

The unit is available in a range of temperature and shock/vibe specifications per ANSI/VITA 47, up to V3 and OS2. The module follows the SOSA specification for its rear I/O to the backplane.

Figure 1: VPX540

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Block Diagram

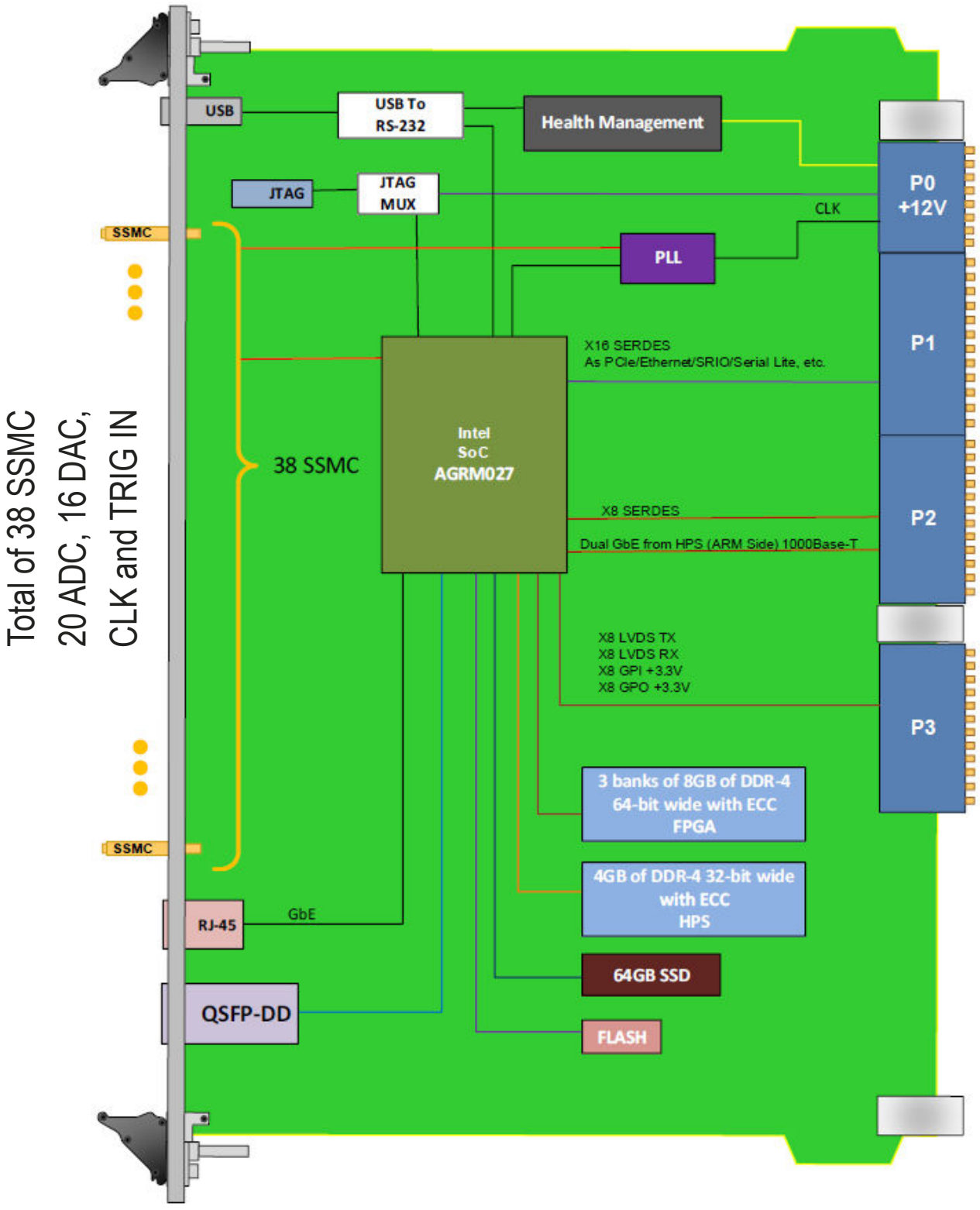

Figure 2: VPX540 Functional Block Diagram

Backplane Pinout

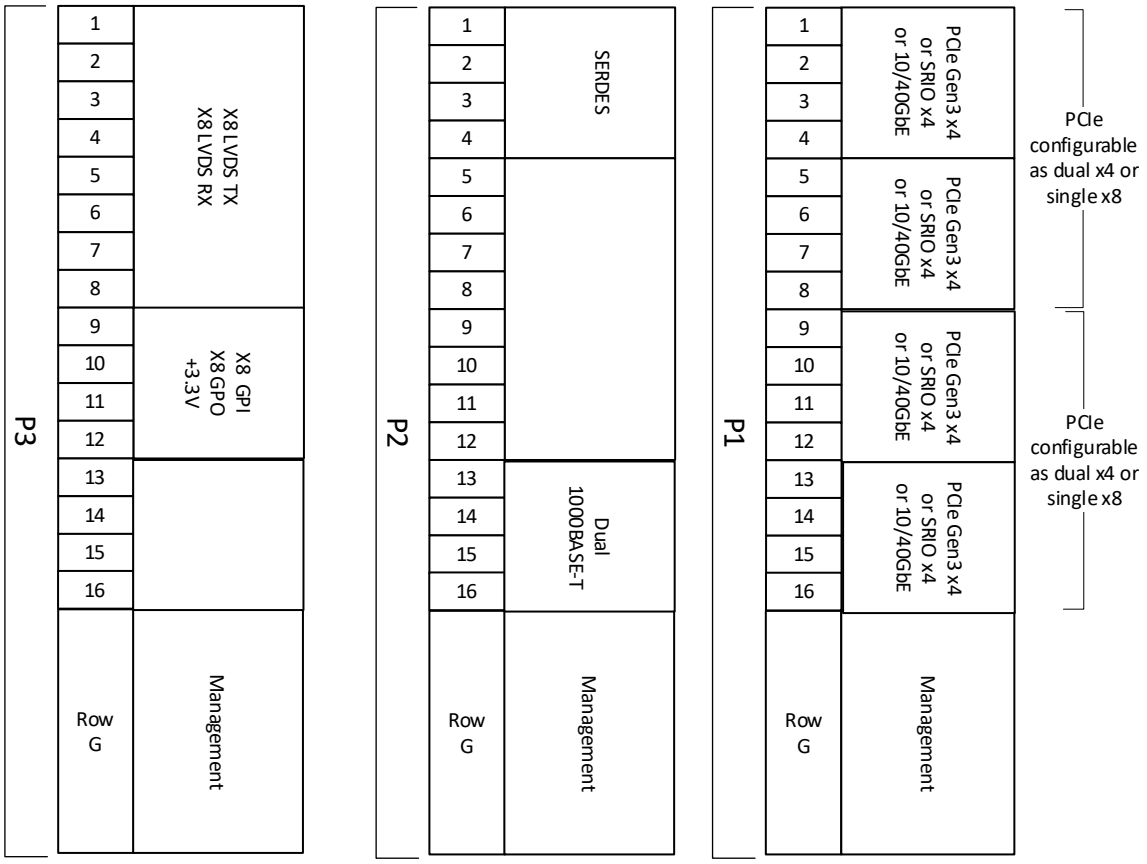

Figure 3: VPX540 Backplane Pinout

Reference Design

VadaTech provides an extensive range of Intel based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high-speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Intel provides RF tool chain into Intel Quartus Prime Software for developing applications on Intel based FPGAs. VadaTech provides reference VHDL developed using the Design Suite for testing hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Intel IP cores, so please contact Intel where these are required.

Intel also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

Software Development Acceleration

Please contact VadaTech for different software packages that are available for the VPX540.

Specifications

Architecture		
Physical	**Dimensions**	6U, 1” pitch
Type	**Controller**	OpenVPX payload module with Health Management
Standards		
VPX	**Type**	VITA 46.x
VPX	**Type**	VITA 46.11
Module Management	**IPMI**	IPMI v2.0
Configuration		
Power	**VPX540**	85W FPGA load dependent
Front Panel	**Interface Connectors**	ADC/DAC input/output via SSMC
		RF Clock via SSMC and Trig in
		RS-232 from FPGA, HPS and from Health Management via USB to RS-232
		1000BASE-T via RJ-45
		QSFP-DD
	LEDs	User defined by the FPGA (8 LED) and Health Management
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	Health Management, Clock on P0
		PCIe, Ethernet, SRIO, Serial Lite on P1/P2
		GbE, GPIO and LVDS on P3
Software Support	**Operating System**	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX540 – ABC-DE0-GHJ

A = RF SoC Part number	D = RF Balun	G = Slot Profile
0 = AGRM027R31D2I2V 1 = AGRM027R31D3I3V*	0 = Anaren 400MHz to 3GHz 1 = Marki 500KHz to 9GHz*	0 = 5 HP, VITA 48.1
B = Optical Transceiver	**E = PCIe on Ports 1 to 16**	**H = Environmental**
0 = None 1 = 40Gb (4x 10G) 2 = 100G (4x 25G) 3 = 200G (4x 50G) 4 = 400G (8x 50G)	0 = None 1 = 1-4 2 = 1-8 3 = 1-12 4 = 1-16 5 = Reserved 6 = Reserved	See Environmental Specification
C = VPX Connector Type		**J = Conformal Coating**
0 = High Speed 50u Gold Rugged High Speed (>25G) 1 = KVPX Connectors		0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic 3 = Parylene

Notes:

* MOQ is required

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes:

*Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX004

- Unified 1 GHz octal-core CPU for, Shelf Manager, and Fabric management
- Automatic fail-over with redundant VPX004
- 1GbE base switch with dual 100/1000/10G uplink

AMC590

- Octal channel high speed ADC
- UltraScale FPGA
- Front panel clock for synchronization

VPX752

- 6U VPX module Intel 5th Generation Xeon-D SoC
- PCIe Gen3 x 16 (dual x8 or Octal x4)
- Octal 10GbE XAUI

VTX870

- Open VPX benchtop development platform
- Dedicated Switch/management slot
- Up to five 6U VPX payload slots

Contact

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