VPX560

Xilinx Zynq-7000, 3U VPX

VPX560

Key Features

- 3U FPGA VPX Module
- AMC Zynq-7000 FPGA in FFG-900 package (XC7Z100 or XC7Z045)
- 256MB of DDR3 32-bit wide to PS
- 512MB of DDR3 64-bit wide to PL
- High-performance clock jitter cleaner
- Protocols such as PCIe, SRIO, 10GbE/40Gbe, etc. are FPGA programmable
- Health Management through dedicated Processor

Benefits

- Reference design with VHDL source code speeds application development
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX560

The VPX560 is an FPGA based on the AMD Zynq-7000.

The FPGA has a single bank of of DDR3 memory (64-bit wide) to the PL side. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host. The FPGA package includes an integrated SoC processor. The processor has a separate single bank of DDR3 (32-bit wide).

The module supports dual GbE as 1000BASE-T to P1 and depending on FPGA code implemented it can support PCIe up to Gen3 (dual x4 or x8 lane), or dual SRIO, 10GbE or 40GbE on P1. There are additional x4 SERDES to each of P1 and P2. The module has x32 GPIO and x8 LVDS which can be configured as x16 single ended. In addition, there are three RS-232 are routed to P2.

The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

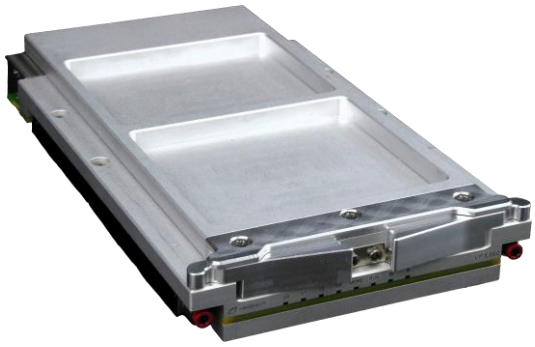

Figure 1: VPX560 (Conduction-Cooled)

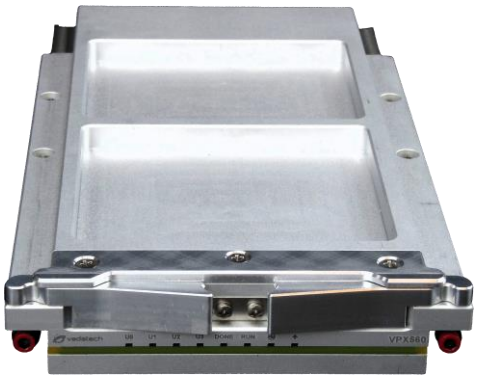

Figure 2: VPX560 Top View (Conduction-Cooled)

Figure 3: VPX560 (PCA only)

Figure 4: VPX560 Front View (PCA only)

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Block Diagram

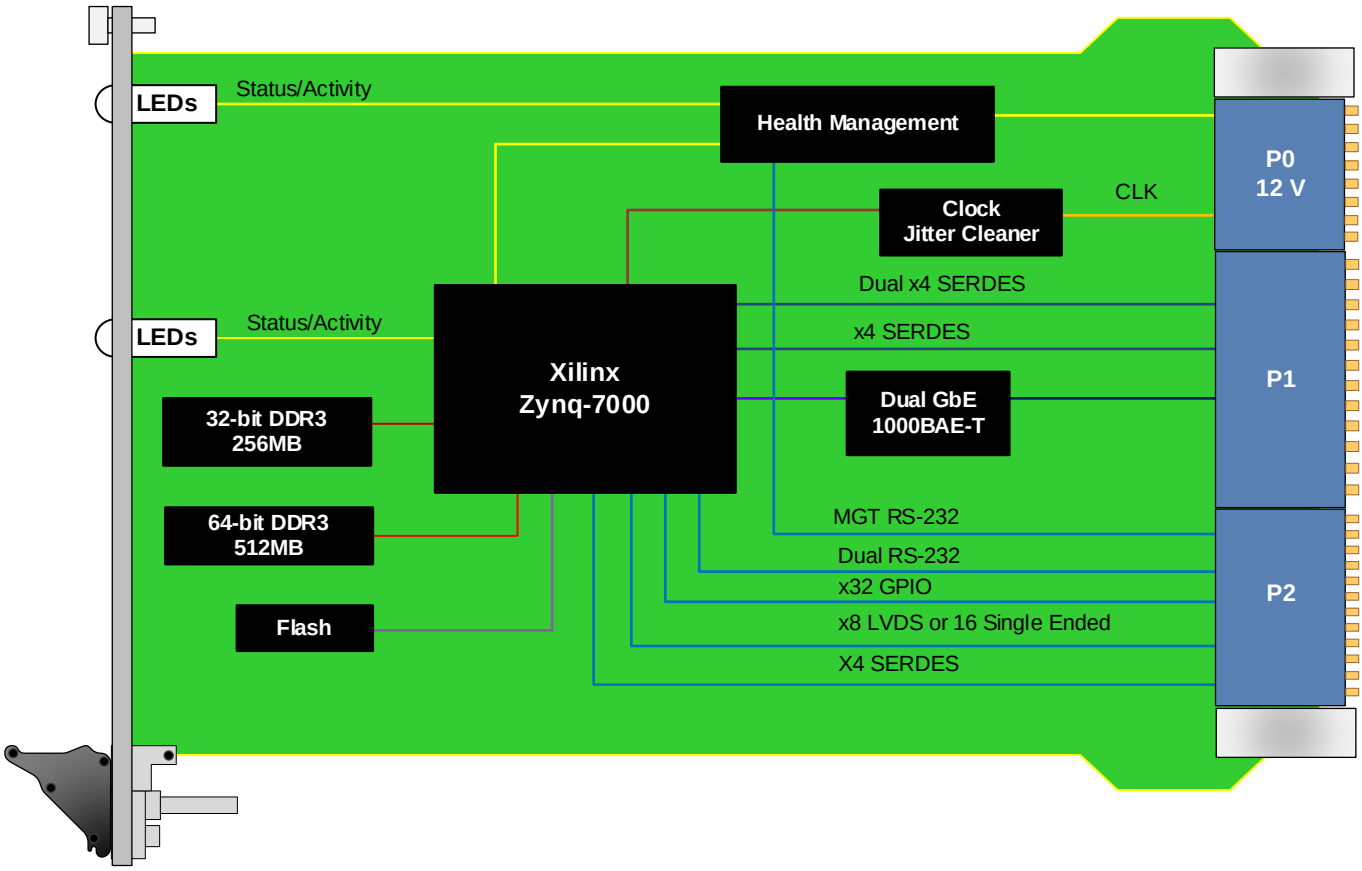

Figure 5: VPX560 Functional Block Diagram

Front panel

Figure 6: VPX560 Front Panel (Conduction-Cooled)

Backplane Pinout

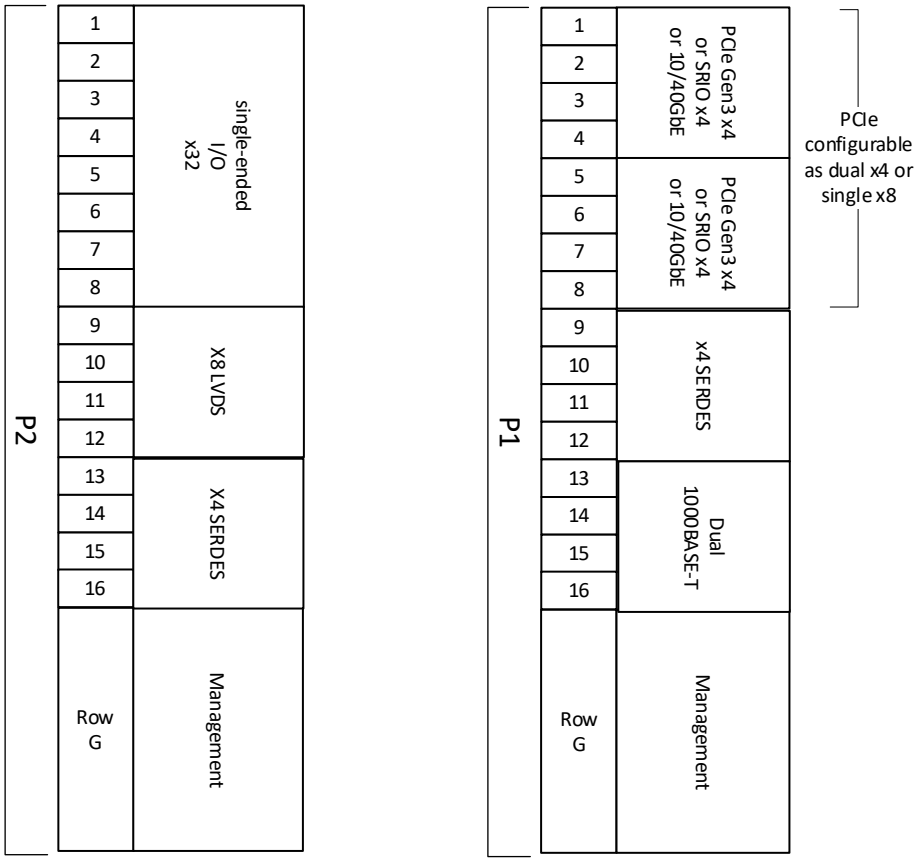

Figure 2: VPX560 Backplane Pinout

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
Configuration		
Power	**VPX560**	~20 W (dependent on FPGA load)
Front Panel	**LEDs**	User defined LEDs from FPGA
	LEDs	Health Management
	LEDs	Link/ACT from the GbE PHY
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	P1: Dual x4 fabric (PCIe Gen3/10GbE/40GbE/SRIO per FPGA load)
		P1: x4 SERDES; Dual GbE 1000BASE-T
		P2: x32 single ended lanes; x8 LVDS; x4 SERDES
	Power Supplies	P0: VS1 = 12V
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX560 – 0BC-DEF-GHJ

	D = FPGA Speed	G = Applicable Slot Profiles
	1 = Reserved 2 = High 3 = Highest	0 = 5 HP
B = VPX Connector Type		**H = Environmental**
0 = Standard 50u Gold Rugged 1 = KVPX Connectors		See Environmental Specification
C = FPGA	**F = PCIe Option (P1) for Data Port 1/2**	**J = Conformal Coating**
0 = Reserved 1 = XC7Z045 2 = XC7Z100	0 = No PCIe 1 = PCIe/None 2 = None/PCIe 3 = PCIe/PCIe	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic 3 = Parylene

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VTX660

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VTX661

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VPX029

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Contact

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