

VPX561

Zynq UltraScale+ FPGA, 3U VPX



VPX561

Key Features

- AMD UltraScale+ XCZU19EG FPGA
- 8 GB of 64-bit wide DDR4 Memory with ECC to PS
- 8GB of 64-bit wide DDR4 Memory to PL
- MPSoC with built-in Block RAM and UltraRAM
- GbE 1000BASE-T to P1 from PS
- Dual GbE to P1 from PS as 1000BASE-BX
- x12 SERDES from PL to P1
- x8 SERDES from PL to P2
- x8 LVDS (can be configured as x16 Single ended) and x16 Singled ended to P2
- Health Management through dedicated Processor

Benefits

- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company



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OpenVPX™



VPX561

The VPX561 is a 3U VPX FPGA based on Zynq Ultrascale+ XCZU19EG MPSoC FPGA. The FPGA has 1968 DSP Slices and 1143k logic cells. The XCZU19EG includes quad-core ARM application processor, dual-core ARM real-time processor and Mali™ graphics processing unit.

The FPGA PL has an interface to a single DDR4 memory channel (64-bit wide) for a total of 8MB and another channel 8MB with ECC to the PS side. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The module has onboard 64 GB of Flash and 128MB of boot Flash.



Figure 1: VPX561



Figure 2: VPX561 PCA View

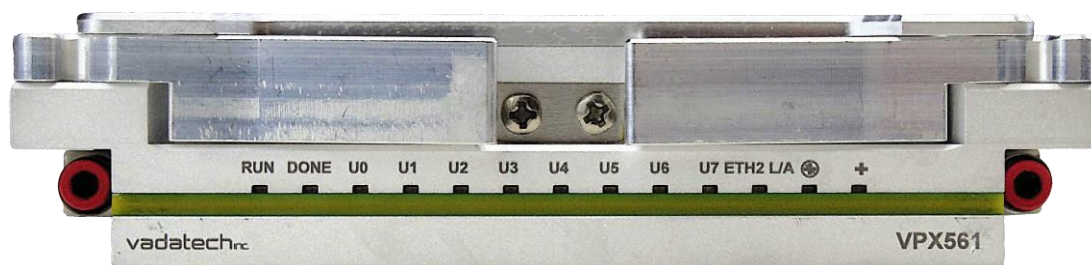


Figure 3: VPX561 Front View

Block Diagram

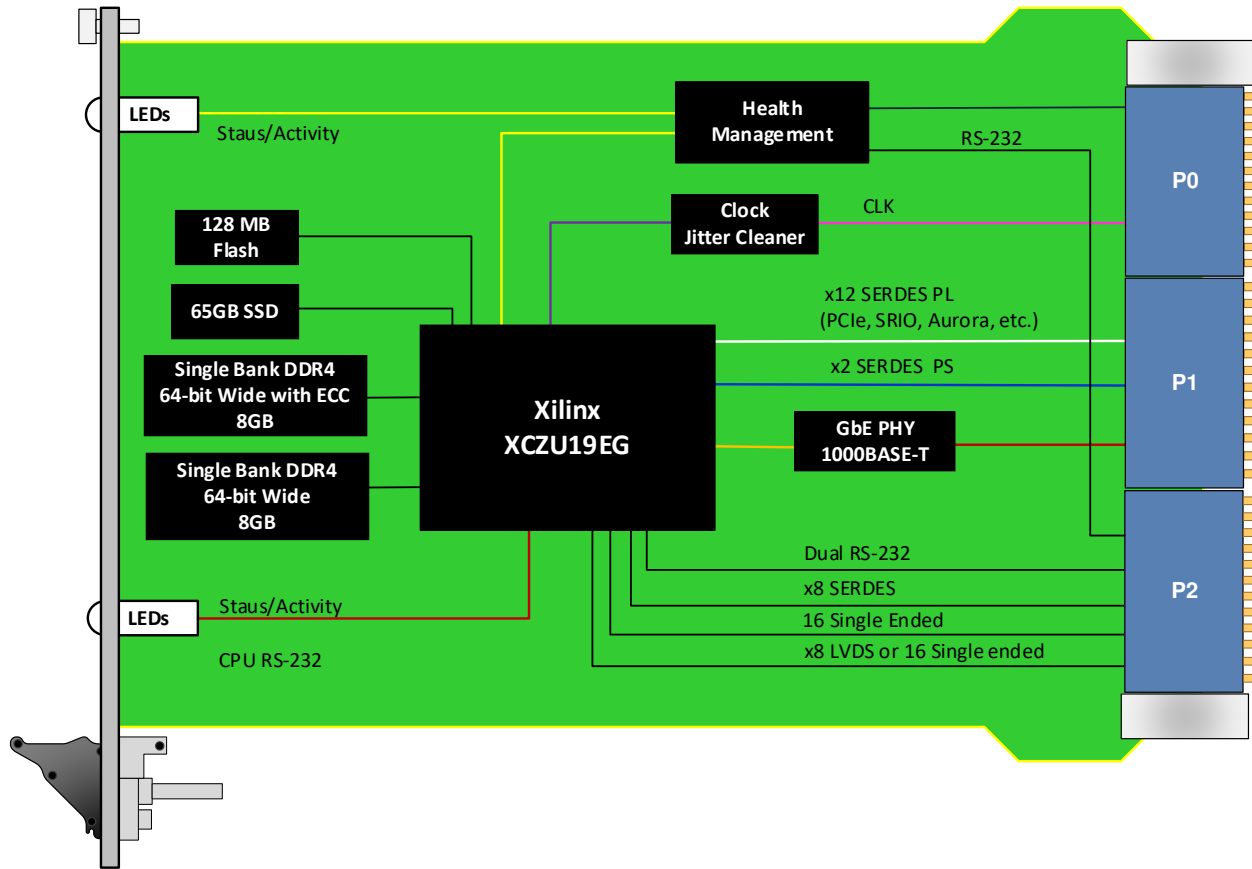


Figure 4: VPX561 Functional Block Diagram

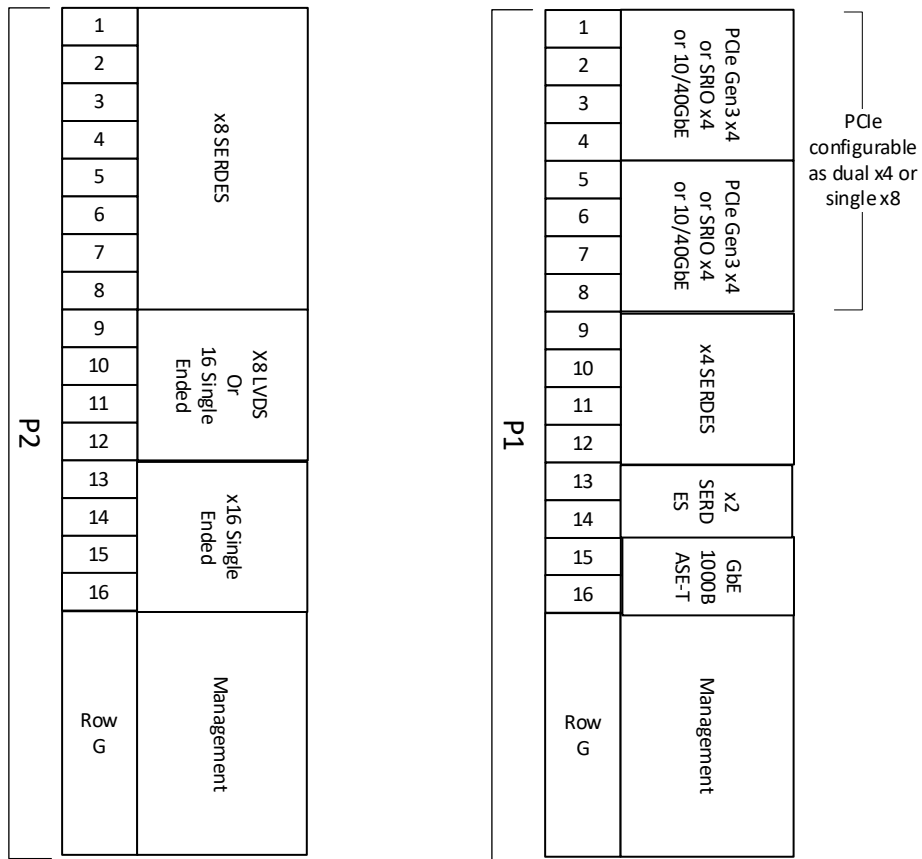


Figure 5: VPX561 Rear Pinout definition

Reference Design

VadaTech provides an extensive range of AMD based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

AMD provides Vivado Design Suite for developing applications on AMD based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or AMD IP cores, so please contact AMD where these are required.

AMD also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

[AMD Vivado Design Suite](#), [AMD System Generator for DSP](#).

Specifications

Architecture		
Physical	Dimensions	3U, 1" pitch
Type	FPGA	AMD Zynq UltraScale+
Configuration		
Power	VPX561	~30W FPGA load dependent
Front Panel	Interface Connectors	Via P1 and P2
	LEDs	Health Management
	LEDs	User defined by the FPGA and status
VPX Interfaces	Slot Profiles	See Ordering Options
	Rear IO	CLK on P0
		x8 SERDES (VITA 46.3, 46.4, 46.7) to P1 (any protocol)
		x4 SERDES to P1 from PL (any protocol)
		x2 SERDES to P1 from PS (GbE)
		GbE 1000BASE-T to P1
		x8 SERDES to P2 from PL (any protocol)
		8 x LVDS on P2 (or configurable as single ended) with additional x16 Single ended
Software Support	Operating System	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX561 – A00-D0F-GHJ

A = VPX Connector Type	D = FPGA Speed	G = Applicable Slot Profiles
0 = Standard 50u Gold Rugged 1 = KVPX Connectors	1 = Reserved 2 = High 3 = Highest	0 = 5HP, VITA 48.1 1 = Reserved
		H = Environmental
		See Environmental Specification
	F = PCIe Option (P1) for lanes 1-4 and 5-8	J = Conformal Coating
	0 = No PCIe 1 = PCIe/None 2 = None/PCIe 3 = PCIe/PCIe	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Notes:

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	H = 0	H = 1	H = 2	H = 3	H = 4
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes:

*Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX592



- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- AMD Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599



- AMD Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

Contact

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