

VPX570

ADC 12-bit @ 5.4 GSPS and
DAC 12-bit @ 6 GSPS, Virtex
UltraScale+, 3U VPX



VPX570

Key Features

- ADC 12-bit @ 5.4 GSPS (EV12AS350A)
- DAC 12-bit @ 6 GSPS (EV12DS460A)
- RF switch to loop the DAC to ADC
- Xilinx UltraScale+ XCVU13P FPGA with 8 GB DDR4
- Supported by development accelerator software package for Multi-Path Modulation
- Health Management through dedicated Processor

Benefits

- Very low latency from ADC to DAC
- XCVU13P has large internal memory
- Reference design with VHDL source code speeds application development
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company



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OpenVPX™



VPX570

The VPX570 provides an ADC with sampling rates of up to 5.4 GSPS at a 12-bit resolution (EV12AS350A) and a DAC that delivers update rates of up to 6 GSPS also at a 12-bit resolution (EV12DS460A). Both Converters have parallel interface to the FPGA, avoiding latency associated with serializing/deserializing data.

The XCVU13P FPGA has large 360 Mb on-chip UltraRAM which, with the ADC and DAC selection, makes this module ideal for low-latency applications such as DRFM, radar simulators and smart jammers. The FPGA interfaces directly to rear I/O via SERDES and LVDS, supporting PCIe, SRIO, GbE/10GbE/40GbE or Aurora backplane connections. General purpose I/O signals, e.g. for trigger, are routed to the front panel that also contains 8 LED/Bi-color.

ADC and DAC have a common sampling clock, which can be fed from front panel (Direct RF Clock) or from PLL locked to a 10/100 MHz reference clock sourced from front panel or backplane. Sampling clock selection is by ordering option.

The module also has an RF Switch which is controlled by the FPGA which allows the DAC output to be routed to the ADC for any kind of calibration.

The VPX570 includes platform health management/monitoring capability using VadaTech's field-proven IPMI software. An onboard management controller has the ability to access board sensors and manage FPGA image updates.

The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

VadaTech's Multi-Path Modulation software package can provide an additional FPGA image and source code for the VPX570, See Datasheet [MPM_VPX570](#) and Video [MPM570 Development Accelerator](#) for details.



Figure 1: VPX570

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

[Xilinx Vivado Design Suite](#), [Xilinx System Generator for DSP](#).

Software Development Acceleration

VPX570 comes bundled with a software license for MPM-VPX570, additional FPGA image and source code to accelerate the development of applications requiring multi-path loop back from ADC to DAC. This code implements programmable delay, and phase and amplitude modulation, across multiple signal paths, combining the result for output to the DAC. A Matlab® model of the code is included to support development.

See [MPM-VPX570](#)

Block Diagram

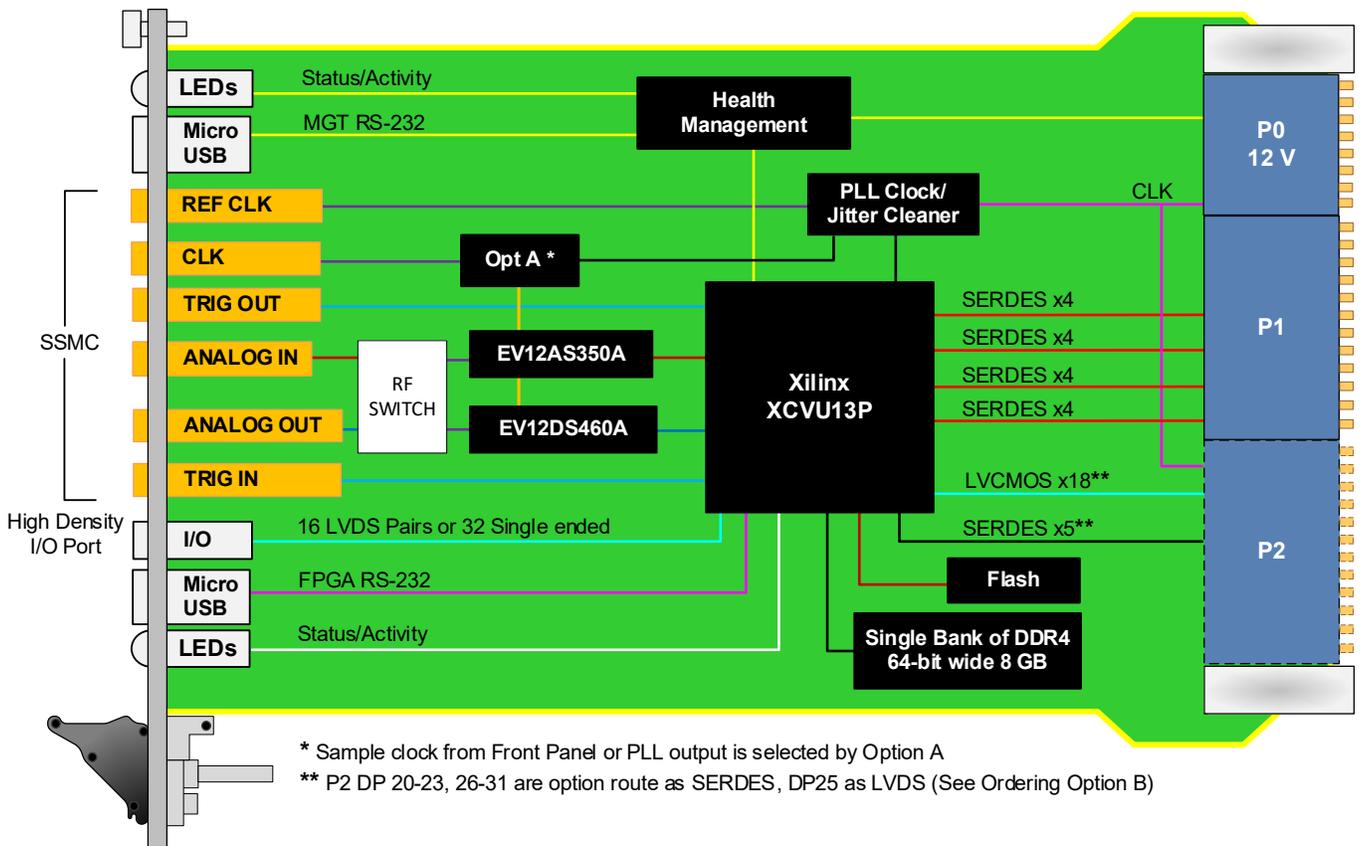


Figure 2: VPX570 Functional Block Diagram

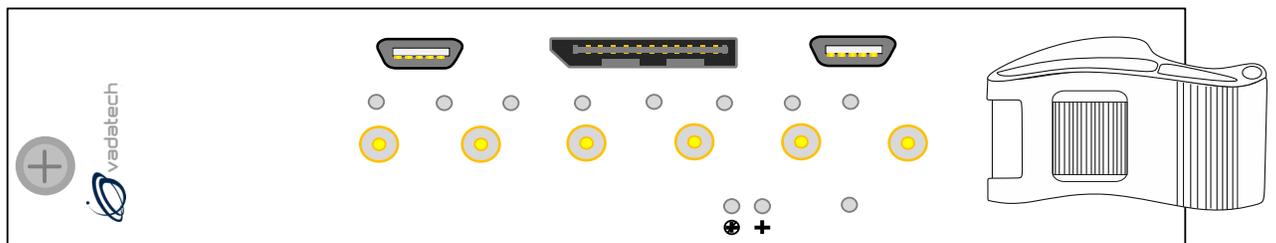


Figure 3: VPX570 Front Panel

Interface	Function	Note
REF CLK	Reference Clock Input	10 MHz to 100 MHz, 50 Ohm, 0 dBm to +10 dBm
CLKIN	Sampling Clock Input	up to 6 GHz, 50 Ohm, +10 dBm to +13 dBm
ANALOG IN	RF Input	50 Ohm, AC coupled, FS input level 8.5 dBm \pm 1 dB Full power -3 dB input BW: 1 MHz to 5.7 GHz
ANALOG OUT	RF Output	50 Ohm, AC coupled, FS output level -3.5 dBm \pm 1 dB Full power -3 dB output BW: 1 MHz to 5.7 GHz
TRIG IN	Trigger Input	0 to 2.5V @ 50 Ohm
TRIG OUT	Trigger Output	0 to 2.5V @ 50 Ohm

Table 1: VPX570 Front Panel Interfaces

Conn.	Name	Standard	Notes
J1		CML	Combination of Fat Pipe, Thin Pipe and Ultra-Thin Pipe Fabric(s) defined by FPGA load and option F TX pairs: P1-DP1, P1-DP3, P1-DP5 ... P1-D31 RX pairs: P1-DP0, P1-DP2, P1-DP4 ... P1-D30
J2 (optional)	REF_CLKO+/- REF_CLKI+/-	LVDS	Reference clock daisy chain (10MHz) REF_CLKI pair: P2-PD1 REF_CLKO pair: P2-DP2
	DP [4:19] +/-	LVC MOS18	16 LVC MOS signal pairs (e.g. to RTM)
	DP24+/-	LVDS	Input/Output pair (FPGA configurable): P2-DP24
	DP25+/-	LVDS	Input/Output pair (FPGA configurable): P2-DP24 (option load)
	DP [20-23] [26-31]	SERDES	Input/Output pair: P2-DP [20-23] [26-31] (option load)

Table 2: VPX570 Backplane Interfaces

Backplane Pinout

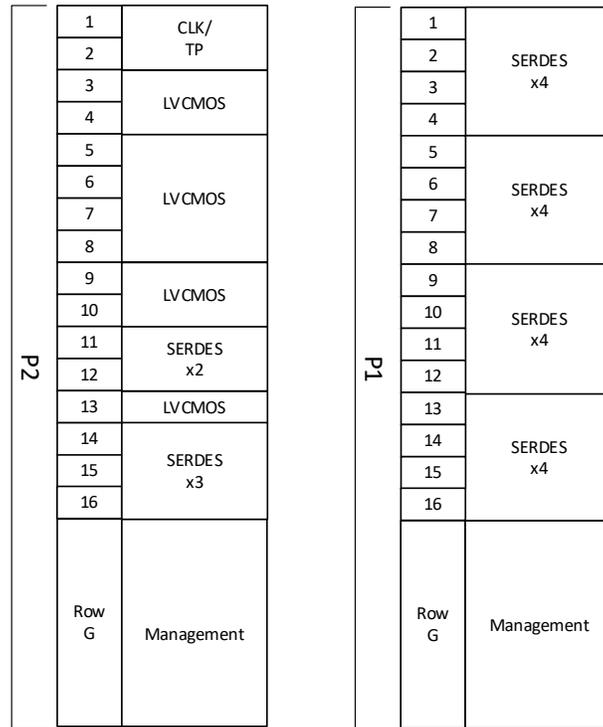


Figure 4: VPX570 Backplane Pinout

Specifications

Architecture		
Physical	Dimensions	3U, 1" pitch
Type	Controller	OpenVPX payload module with Health Management
Standards		
VPX	Type	VITA 46.x
VPX	Type	VITA 65 OpenVPX
Module Management	IPMI	IPMI v2.0
Configuration		
Power	VPX570	65W FPGA load dependent
Front Panel	Interface Connectors	General purpose I/O Analog input Analog output Clock
	Micro USB	RS-232 from FPGA and RS-232 from Health Management
	LEDs	User defined by the FPGA (8 LED/Bi-color) and Health Management
VPX Interfaces	Slot Profiles	See Ordering Options
	Rear IO	Health Management, Clock on P0 SERDES on P1 (can be mix of GbE, PCIe, SRIO, XAUI, Aurora) LVDS and SERDES on P2
Software Support	Operating System	Agnostic
Other		
MTBF		MIL Hand book 217-F@ TBD hrs
Certifications		Designed to meet FCC, CE and UL certifications, where applicable
Standards		VadaTech is certified to both the ISO9001:2015 and AS9100D standards
Warranty		Two (2) years, see VadaTech Terms and Conditions

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX570 – ABC-DEF-GHJ

A = RF Direct Clock Sampling 0 = Direct RF Clock 1 = Onboard Wideband PLL	D = FPGA Speed 1 = Reserved 2 = High 3 = Highest	G = Slot Profile 0 = 5 HP, IEEE 1101
B = P2 SERDES/LVDS 0 = No SERDES on P2DP (20-23, 26-31) and No LVDS on P2DP 25 1 = SERDES on P2DP (20-23, 26-31) and LVDS on P2DP 25	E = VPX Connector Type 0 = Standard 50u Gold Rugged 1 = KVPX Connectors	H = Environmental See Environmental Specification
C = Backplane P2 0 = P2 fitted 1 = P2 not fitted	F = PCIe Option (P1) for Data Port 1/2/3/4 0 = No PCIe* 1 = PCIe x4 on DP0* 2 = PCIe x8 on DP0/1* 3 = PCIe x16 on DP0/1/2/3	J = Conformal Coating 0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Notes:
 *SERDES lanes that are not PCIe can be used for SRIO, XAUI or Aurora, with combination of FP, TP and UTP depending on FPGA image.
 For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

Option H	Air Cooled			Conduction Cooled		
	H = 0	H = 1	H = 2	H = 3	H = 4	
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)	
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)	
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)	
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)	
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	

Notes:
 *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX004



- Unified 1 GHz quad-core CPU for, Shelf Manager, and Fabric management
- Automatic fail-over with redundant VPX004
- 1GbE base switch with dual 100/1000/10G uplink

VPX752



- 6U VPX module Intel 5th Generation Xeon-D SoC
- PCIe Gen3 x 16 (dual x8 or Quad x4)
- Quad 10GbE XAUI

VTX870



- Open VPX benchtop development platform
- Dedicated Switch/management slot
- Up to five 3U VPX payload slots

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